CURRICULUM AND SYLLABI

M.Tech.

in

ELECTRONICS DESIGN AND TECHNOLOGY

(With effect from Academic Year 2018-2019)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY CALICUT

CALICUT - 673601

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

National Institute of Technology Calicut

Vision of the Department of Electronics and Communication Engineering:

The Department of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering.

Mission of the Department in pursuance of its vision:

The mission of the Department of Electronics and Communication Engineering is to impart high quality technical education by offering undergraduate, graduate and research programs in the domain of Electronics and Communication Engineering with thorough foundation in theory along with strong hands-on design and laboratory components, tools and skills necessary for the students to become successful major contributors to society and profession.

Programme Educational Objectives (PEOs) and Programme Outcomes (POs): PG Course in Electronics Design and Technology

Programme Educational Objectives (PEOs)

Sl. No.	Program Educational Objectives
PEO 1	To produce graduates with a solid foundation in Electronics Engineering fundamentals including hardware, software and mathematics and make them competent to apply this knowledge in their chosen career in the electronics design industry.
PEO 2	To ensure that graduates will be proficient in analyzing real life problems with high sensitivity to the needs of society, and provide solutions which are economically and socially feasible.
PEO 3	To produce graduates who have the necessary competence and innovative skills to be an effective part of the research field of electronics design and development.
PEO 4	To produce graduates who are adequately motivated to continue in their chosen field and build greater technical knowledge and develop higher skills as technology advances and changes.

Programme Outcomes (POs) & Programme Specific Outcomes (PSOs) of M.Tech.in Electronics Design and Technology

PO1	An ability to independently carry out research /investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report/document
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PSO1	Inculcate the ability to understand clearly the steps in designing electronic systems which are in tune with current technology and adaptable for future changes
PSO2	Create an environment such that graduates develop a passion for hardware and software design and be part of the electronic design industry to become leaders in indigenous product development

Curriculum for M. Tech. in Electronics Design and Technology

Semester 1

Sl.No	Code	Title	L	T	P	C
1	EC6101D	Digital System Design using HDL	3	0	2	4
2	EC6102D	Embedded System Design	3	0	2	4
3	EC6103D	Mathematical Techniques for Electronics Design	4	0	0	4
4		Elective 1	3	0	0	3
5		Elective 2	3	0	0	3
		Total credits				18

Semester 2

Sl.No	Code	Title	L	T	P	C
1	EC6104D	Electromagnetic Compatibility	4	0	0	4
2	EC6105D	Electronics Product Design	1	0	3	3
3	EC6106D	Seminar	0	0	2	1
4		Elective 3	3	0	0	3
5		Elective 4	3	0	0	3
6		Elective 5	3	0	0	3
		Total credits				17

Semester 3

Sl.No	Code	Title	L	T	P	C
1	EC7101D	Project-Part 1	0	0	24	12
		Total credits				12

Semester 4

Sl.No.	Code	Title	L	T	P	C
1	EC7102D	Project-Part 2	0	0	26	13
		Total credits				13

Elective Courses

Sl.No	Code	Title	L	T	P	C
1	EC6121D	Advanced Embedded Computing	3	0	0	3
2	EC6122D	Real Time Operating System	3	0	0	3
3	EC6123D	Advanced Processor Architecture	3	0	0	3
4	EC6124D	Design for Manufacturability	3	0	0	3
5	EC6125D	DSP System Design	3	0	0	3
6	EC6126D	Networking and IoT	3	0	0	3
7	EC6127D	Mechatronics	3	0	0	3
8	EC6128D	Biomedical Instrumentation	3	0	0	3
9	EC6129D	Analog and Data Conversion Systems	3	0	0	3
10	EC6130D	Control System Design	3	0	0	3
11	EC6131D	Artificial Intelligence	3	0	0	3
12	EC6132D	Data Structures and Algorithms	3	0	0	3
13	EC6133D	Electronic Packaging	3	0	0	3
14	EC6211D	MOS Device Modelling	3	0	0	3
15	EC6213D	Digital VLSI Testing	3	0	0	3
16	EC6214D	VLSI Digital Signal Processing	3	0	0	3
17	EC6217D	MEMS Structures and Applications	3	0	0	3
18	EC6219D	High Speed Digital Design	3	0	0	3
19	EC6220D	Low Power VLSI	3	0	0	3
20	EC6224D	Verification of VLSI Systems	3	0	0	3

Notes:

- The minimum number of total credits to be earned by a student for the award of the degree is 60. The total credits must not exceed 62.
- A minimum of three elective courses must be credited from the list of electives given for the specialization. A maximum of two electives can be credited from any other specializations, offered by the institute at M.Tech. level, with the consent of the HOD, the Programme Coordinator and the Course Faculty without exceeding the maximum credits allowed.

Syllabus for M. Tech. in Electronics Design and Technology

CORE COURSES

EC6101D DIGITAL SYSTEM DESIGN USING HDL

Pre-requisites: Nil

L	T	P	C
3	0	2	4

Total hours: 39 L+26 P

Module 1: (13 hours)
Introduction to digital design methodology using HDL–RTL design using Verilog – Verilog language concepts – data types and operators – structural, data flow and behavioral models -hierarchical structure – combinational and sequential circuit description - continuous and procedural assignments - blocking and non-blocking assignments -tasks and functions - delay modeling – parameterized reusable design – system tasks - design verification using test benches – compiler directives.

Module 2: (13 hours)
Datapath and controllers – complex state machine design – modeling FSM in verilog – modeling memory – basic pipelining concepts – pipeline modeling – User defined primitives – switch level modeling - implementation of arithmetic functions – adder, multiplier, divider, square root.

Impediments to Synchronous design: Clock Skew, Gating the clock, Asynchronous inputs, Synchronizer Failure and Metastability: Synchronizer failure, Metastability Resolution Time, Reliable Synchronizer Design, Analysis of Metastable timing, Metastable hardened flip flops, Synchronizing High Speed data transfers.

Module 3: (13 hours)
Introduction to synthesis - Logic Synthesis - RTL Synthesis - High-Level Synthesis, Synthesis of Combinational Logic - Synthesis of Priority Structures - Exploiting Logical Don't-Care Conditions, Synthesis of Sequential Logic with Latches and Flip-flops – accidental and intentional latches – synthesis of state machines – registers and counters – clocks – loops - code optimizations – design examples.

Programmable LSI Techniques - Programmable Logic Arrays - Programmable Array Logic - PLDs - Complex Programmable Logic Devices and Field Programmable Gate Arrays –Xilinx/Altera Series FPGAs – Programmable System on Chip – Zynq SoC design overview – prototyping on FPGA.

References:

1. Ciletti M.D.,*Advanced digital design with the Verilog HDL*, Second Edition, Prentice Hall, 2010.
2. Charles Roth, Lizy Kurian John, ByeongKil Lee, *Digital systems design using Verilog*, First Edition,
   Cengage Learning, 2014.
3. John F Wakerley,*Digital Design Principles and Practice*, Fourth Edition, Pearson education, 2008
4. J. Bhasker, *Verilog HDL Synthesis: A Practical Primer*, B. S. Publications, 2001.
5. Crockett LH, Elliot RA, Enderwitz MA, Stewart RW, *The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc*, Strathclyde Academic Media, 2014.

EC6102D EMBEDDED SYSTEM DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	2	4

Total hours: 39 L+26 P

Module 1: (16 hours)
Introduction to Embedded system, Embedded system examples, Typical MCU - Power supply, clock, GPIO,timer/counter, WDT, Stack, Interrupts, DMA. Memory Technologies – SRAM, DRAM, SDRAM, EPROM,Flash. Low power design. Pull up/Pull down resistors- switch interface. Sensors-temperature, Light, humidity, pressure, etc. Actuators-LED, displays, Motors, Relays, etc. ADC/DAC interfacing.

Embedded programming – IDE, Compiler/Assembler, Simulator/Emulator. Buses& Protocols – I2C, SPI, UART, USB, CAN, AMBA. Ethernet/WLAN/Bluetooth/Zigbee.

Module 2: (13 hours)
ARM architecture, ARM organization and Implementation, Memory Hierarchy, ARM Instruction Set and Thumb Instruction set, Assembly Language Programming, High- Level Language Programming.

Peripheral Programming and system design for a specific ARM processor (ARM 7/9/11/Cortex)

Digital Signal Processors- General Features. SIMD – Black fin/SHARC. TMS320 family of DSPs/ OMAP. Application scenario of DSP processors.

Module 3: (10 hours)
Operating systems- history,types. Layers of an OS. OS- Functions, Thekernel, Task/Process, Thread, InterProcessCommunication, Task synchronization,Semaphores,Priority inversion,Device drivers.Various Scheduling algorithms -Preemptive/Non preemptive methods.

RTOS. Types of Real time tasks.OS for embedded systems. Qualities of Good RTOS. Real time scheduling algorithms -Offline/Online-RM /EDF algorithms.

References:

1. Lyla.B.Das,*Embedded Systems, An Integrated Approach*, Pearson Ed, 2013
2. Shibu K.V. *Introduction to Embedded Systems* Tata McGraw Hill, 2009
3. William Hohl, *ARM Assembly Language Programming* CRC Press,2009
4. Abraham Silberschatz,Peter Baer Galvin and Greg Gagne*, Operating System Concepts*, 7th Edition Wiley Higher Education, 2005
5. Hermann Kopetz: *Real-time systems: design principles for distributed embedded applications*, Kluwer academic publishers, 2002

EC6103D MATHEMATICAL TECHNIQUES FOR ELECTRONICS DESIGN

Pre-requisites: Nil

L	T	P	C
4	0	0	4

Total hours: 52
Module 1: (20 hours)

Linear Algebra: Vector spaces, Subspaces, Basis and Dimension, Inner product spaces, Gram-Schmidt orthogonalization, Orthonormal bases, Linear transformations, Kernels and images, Matrix representation of linear transformation, Change of basis, Eigenvalues and eigen vectors of linear operator, Quadratic form, Singular value decomposition.
Signal Space:Signals and vectors, inner product of signals, norm- notion of length of signal and distance between signals, orthogonal signal space, Fourier series representation, Fourier transform, power spectral density and energy spectral density

Module 2: (16 hours)

Random Variables: Probability axioms, Conditional probability, Discrete and continuous random variables, Expected value, Variance, Functions of a random variable, Functions of multiple random variables, Independent/uncorrelated random variables, Moment generating function, Sample mean, Laws of large numbers, Central limit theorem. Introduction to random processes, Mean and correlation of random processes, Stationary, wide sense stationary and ergodic processes.

Module 3: (16 hours)

Linear Programming: Introduction, Optimization model, Formulation and applications, Classical optimization techniques: single and multi-variable problems, Types of constraints, Linear optimization algorithms: Graphical method, Simplex method, Basic solution and extreme point, Degeneracy, Primal simplex method,Dual linear programs, Duality theory, Dual simplex method, Primal-dual algorithm.

References:

1. Gareth Williams, *Linear Algebra with Applications*, Jones and Bartlett Publishers, 6thEdn., 2008.
2. Gilbert Strang*, Introduction to Linear Algebra*, SIAM, 5thEdn., 2016.
3. A. Papoulis and S. U. Pillai, Probability, *Random Variables and Stochastic Processes*, McGraw Hill, 4thEdn, 2002.
4. V. Krishnan, *Probability and Random Processes*, John Wiley & Sons, 2ndEdn. 2006.
5. Hamady A Taha, *Operation Research: A Introduction*, Pearson, 9th Edn., 2013
6. Igor Griva, ArielaSofer, Stephen G. Nash, *Linear and Nonlinear Optimization*, SIAM, 2009.

EC6104D ELECTROMAGNETIC COMPATIBILITY

Pre-requisites: Nil

L	T	P	C
4	0	0	4

Total hours: 52

Module 1: (18 hours)
Need for Electromagnetic Compatibility, Two aspects of EMC – Emission and Susceptibility, Radiation and Conduction, Designing for EMC, EMC regulations, designing for Electromagnetic Compatibility.

Noise and Interference, Typical Noise path, Methods of noise coupling, Non-ideal behavior of electronic components

Capacitive and Inductive Coupling, Effect of Shielding on capacitive and inductive coupling, Shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, Shield Transfer Impedance -shielding properties of various cable configurations, coaxial cable and shielded twisted pair, braided shields, ribbon cables, Shield Terminations

Safety grounds, signal grounds, single point, multi-point and hybrid grounds, Chassis Grounds, Common Impedance Coupling, Grounding of cable shields, Ground loops and its breaking, Common Mode Choke – Analysis at low and high frequencies, Balancing and Filtering

Module 2: (17 hours)

Digital circuit grounding, internal noise sources, Digital circuit ground noise, minimizing ground impedance and loop area, ground grid, ground plane, Ground plane current distribution, ground plane impedance. Current flow in micro-strip and strip-line routing

Digital circuit power distribution- Transient power supply currents, decoupling capacitor design, effective decoupling strategies, decoupling capacitor selection and mounting

Radiated emission - Differential mode and common mode radiation – Reasons and controlling methods,

Conducted emission – Power line impedance, Line impedance stabilization network, Common mode and differential mode noise sources in SMPS. Power line filters,

Module 3: (17 hours)

PCB layout and stack up - General PCB layout Considerations, PCB to chassis ground connections, return path discontinuity, PCB layer stack up, General PCB design procedure, mixed signal PCB layout, Split planes, Ground connection and power distribution, vertical isolation

Near fields and far fields, characteristic and wave impedances, shielding effectiveness, absorption and reflection loss, shielding with magnetic material, apertures, conductive gaskets, conductive windows, conductive coating, grounding of shields.

Electrostatic Discharge (ESD) -Static generation, human body model, static discharge, ESD protection in equipment design, Transient and Surge Protection Devices, ESD grounding, non-grounded products, software and ESD protection, ESD versus EMC, ESD Testing

References:

1. Henry W.Ott, *Electromagnetic Compatibility Engineering*, John Wiley & Sons, 2009

2. Henry W.Ott, *Noise Reduction Techniques in Electronic Systems*, Second Edition Wiley Interscience Publication, 1988
3. Clayton R.Paul, Introduction to Electromagnetic Compatibility, Second Edition , Wiley Interscience Publication,2006
4. V. Prasad Kodali, *Engineering Electromagnetic Compatibility-Principles, Measurements, Technologies, and Computer Models* Second Edition IEEE Press, 2001
5. Ralph Morrison*, Grounding and Shielding circuits and interference* 5th edition Wiley,2007

EC6105D ELECTRONICS PRODUCT DESIGN

Pre-requisites: Nil

L	T	P	C
1	0	3	3

Total hours: 13L+39P

Lecture :(13 hours)

Product development life cycle – various life cycle models. Aesthetics in a product design. Ergonomics. Design for Reliability – failures and solutions. Design for Manufacturability. PCB design – design rules, Schematics, creating Gerber files, etc. Electrical testing of the system. Familiarizing various tools – Shop bot, 3D printer, Laser cutter, PCB fabrication machine & soldering tools.

Practical: (39 hours)

The students need to implement the prototype model of an electronic product undergoing different stages of product development life cycle, which include:

- Requirements/market study/feasibility study
- Finalizing the Specifications
- Mechanical design
    - Ergonomics and Aesthetics
- Hardware Design
    - Component selection
    - Schematic Entry
    - Layout Design
    - PCB manufacturing and assembly
- Assembly
- Software Design
- Testing.

References:

1. V.B. Baru R.G.Kaduskar, *Electronic Product Design*, Wiley India 2011
2. Tony Ward and James Angus, *Electronic Product Design*, Chapman &Hall 1996

EC6106D SEMINAR

Pre-requisites: Nil

L	T	P	C
0	0	2	1

Total Hours: 26P

The objective of the seminar is to impart training to the students in collecting materials on a specific topic in the broad domain of Engineering/Science from books, journals and other sources, compressing and organizing them in a logical sequence, and presenting the matter effectively both orally and as a technical report. The topic should not be a replica of what is contained in the syllabi of various courses of the M.Tech program. The topic chosen by the student shall be approved by the Faculty-in-Charge of the seminar. The seminar evaluation committee shall evaluate the presentation of students. A seminar report duly certified by the Faculty-in-Charge of the seminar in the prescribed form shall be submitted to the department after the approval from the committee.

EC7101D PROJECT- PART 1

Pre-requisites: Nil

L	T	P	C
0	0	24	12

Total Hours: 312P

The major project in the third and fourth semesters offers the opportunity to apply and extend the knowledge acquired in the first year of the M. Tech. program. The major project can be analytical work, simulation, hardware design or a combination of these in the emerging areas of Electronics Design and Technology, under the supervision of a faculty from the ECE Department. The specific project topic undertaken will reflect the common interests and expertise of the student(s) and supervisor. Students will be required to1) perform a literature search to review current knowledge and developments in the chosen technical area; 2) undertake detailed technical work in the chosen area using one or more of the following:

- Analytical models
- Computer simulations
- Hardware implementation

The emphasis of the major project shall be on facilitating student learning in technical, project management and presentation spheres. The project work will be carried out individually. The M. Tech. project evaluation committee of the department shall evaluate the project work during the third semester in two phases. The first evaluation shall be conducted in the middle of the semester. This should be followed by the end semester evaluation. By the time of the first evaluation, students are expected to complete the literature review, have a clear idea of the work to be done, and have learnt the analytical / software / hardware tools. By the time of the second evaluation, they are expected to present the results of their advancements in the chosen topic, write an interim technical report of the study and results, and clearly state the work plan for the next semester.

EC7102D PROJECT- PART 2

Pre-requisites: Successful completion of EC 7101D PROJECT-PART 1

Total Hours: 338P

L	T	P	C
0	0	28	13

Syllabus

EC7102D Project- Part 2 is a continuation of EC7101D Project: Part 1 of the third semester. Students should complete the work planned in the third semester, attaining all the objectives, and should prepare the project report of the complete work done in the two semesters. They are expected to communicate their innovative ideas and results in reputed conferences and/or journals. The M. Tech. project evaluation committee of the department shall evaluate the project work during the fourth semester in two phases. The first evaluation shall be conducted towards the end of the semester. This should be followed by a second evaluation by the committee including an external examiner.

ELECTIVE COURSES

EC6121D ADVANCED EMBEDDED COMPUTING

Pre-requisites:Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (13 hours)

Architecture of Intel processors from 80286 to Pentium-Microarchitectural techniques of advanced processors –pipelining-superscalar concept –Out of order execution –Speculative execution – branch prediction –register renaming -Multicore processors- Processors beyond Pentium- Architecture of ARM Cortex-M – NVIC – WIC--Sleep modes – peripheral programming of a Cortex-M processor.

Module 2: (13 hours)

Robotics – Designing robotics applications using ARM cortex-M in MSP 432 Robotics kit GPU Processing

M2M to IoT – A Market Perspective – Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT. M2M to IoT- An Architectural Overview – Building architecture, Main design principles and needed. An IoT architecture outline, standards considerations. Review of internet protocols –Processing platforms for IoT-sensors – actuators-Cloud computing models.

Module 3: (13 hours)

Low power, low range protocols –Zigbee –BLE – 6LoWPAN. Applications for IoT-Smart home, city, agriculture etc, - IoT services Project work on Design and development of an IoT product

Linux and linux device drivers –Linux Internals-Project work on porting a real time OS onto an embedded board

References:

1. Lyla B. Das, *The x86 Microprocessors: 8086 to Pentium,, Multicores, Atom , and the 8051 Microcontroller : Architecture ,Programming and Interfacing*, Second Edition , Pearson Education ,India 2014
2. Lyla B. Das, *Architecture, Programming, and Interfacing of Low-power Processors – ARM7, Cortex-M*, Cengage, 2017
3. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, *From Machine-to-Machine to the Internet of Things*: *Introduction to a New Age of Intelligence*, 1st Edition, Academic Press, 2014.
4. ArshdeepBagha, Vijay Madisetti , *Internet of Things ,A hands on approach*,2015
5. Daniel P. Bovet, Marco Cesati, *Understanding the Linux Kernel*, 3rd Edition, O'Reilly,2005

EC6122D REALTIME OPERATING SYSTEMS

Pre-requisite: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (13 hours)

Overview of Operating Systems-Process management-memory Management –Kernel data structure-Computing Environments –Open source Operating Systems- System calls-Process management – Scheduling algorithms-Non-premptive-Co-operative –Shortest Job First-Priority based – Preemptive algorithms- Round robin-Shortest Job next- Priority driven-Threads –Real Time Systems- Scheduling using RM algorithm and EDF algorithm

Module 2: (13 hours)

Inter-process Communications-Pipes – mailboxes – message passing- Process Synchronization-Critical section –racing –readers writers' problem- Bounded buffer problem – Mutex and Semaphore – Deadlock management-File system and IO management- Memory management- Segmentation and paging –case study of x86 processors with paging and segmentation.

Module 3: (13 hours)

Protection –goals and implementation- Security –Cryptographical solutions-Virtual machines – Distributed Systems-Case Studies – Linux – and linux device drivers – Practical work using linux.

References:

1. Abraham Silberschatz,,Peter Baer Galvin and Greg Gagne,*Operating System Concepts*, 7th Edition Wiley Higher Education,2005
2. Daniel P. Bovet, Marco Cesati, *Understanding the Linux Kernel*, 3rd Edition, O'Reilly,2005
3. Hermann Kopetz, *Real-time systems: design principles for distributed embedded applications*, Kluwer Academic Publishers, 2002
4. Jane W.S. Liu: *Real -Time Systems*, Pearson Education, 2008

EC6123D ADVANCED PROCESSOR ARCHITECTURE

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (14 hours)

Technology trend -performance measurement –Comparing and summarizing performance-quantitative principles of computer design –Amdahl's law-Case studies. History of the x86 family - Instruction Setarchitecture of a typical advanced x86 processor –80386 to Pentium. Enhancements of 80386,Hardware Features, Protected virtual addressing mode -Virtual Memory, Memory Management Unit, Converting a Logical Address to a Physical Address, Calculating the size of the Logical Address Space, Protection, Multi-Tasking, Interrupts of 80386

Module 2: (13 hours)

The Enhanced Features of 80486, Data Alignment

Instruction level parallelism -Instruction level parallelism and concepts Superscalar -Branch prediction techniques-Overcoming data hazard and dynamic scheduling –dynamic scheduling -examples and algorithm-Hardware based speculation-

Module 3 (12 hours)

The Pentium Processor and Processors beyond Pentium-Latest Trends in Microprocessor Design-multicore processors

ARM Cortex architecture-Cortex-M to M7 –Architecture – NVIC –Advanced features – Practical work in porting an OS to a Cortex board – peripheral programming of Cortex-M boards

References:

1. Hennesy J. L. &Pattersen D. A., *Computer Architecture: A Quantitative approach*, 4/e, Elseiver Publications, 2007
2. Lyla B.Das*The x86 Microprocessors –Architecture Programming and Interfacing -8086 to Pentium*, Pearson Education , 2010
3. Lyla B. Das, *Architecture, Programming, and Interfacing of Low-power Processors – ARM7, Cortex-M*, Cengage, 2017
4. 4. Pattersen D. A. &Hennesy J. L., *Computer Organization and Design: The Hardware/ Software Interface*, 3/e, Elseiver Publisher, 2014
5. John Shenn,*Modern Processor Design: Fundamentals of Superscalar Processors*, McGraw-Hill series in Electrical Engineering, 2002

EC6124D DESIGN FOR MANUFACTURABILITY

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1 (13 Hours):

Product Life cycle – Introduction, Growth, Mature and Saturation, Product life cycle management, What is DFM, Need of DFM – Higher Quality, Lower Cost, Faster Time to market, better Yield etc. Designer vs manufacturer.

Need for different DFM techniques for different companies – Different applications, Different manufactures, Different equipment and processes. Development of DFM rules, Design Guidelines, exceptions.

Simple assembly process vs complex and expensive components, Simple component manufacture vs complex manufacturing process, Simple and inexpensive design vs expensive and complex service and support.

Module 2 (13 Hours):

DFM softwares. Emerging manufacturing trends, Lead free design, standard design processes, Certifications. Over view of Design for Testability, Design for Assembly, Design for serviceability, Design for reliability etc.

PCB Design and manufacturing process. Design considerations for different types of PCBs – Single layer PCBs, Multilayer PCB, Flexible PCB etc. Design considerations for PCBs for different applications – digital circuits, Analog circuits, High speed circuits, Power circuits etc.Layout rules and parameters. Design rule checks – Signal layer checks, Power/Ground checks, Solder mask check, Drill check etc.

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Module 3 (13 Hours):

Manual verification – Thermal design, plane split width, isolation, PCB thickness etc. Automated processes, Through Hole vs SMT technologies. Thermal profiling during SMD/PTH assembly.

Case studies to understand DFM from design, manufacturing and Assembly

Miniaturization and increased complexity of VLSI circuits Functional Yield, Parametric Yield, Reliability, Yield Loss Modules, Yield analysis Higher Yield Cells, Spacing and Width of interconnect wires, Redundancy in the design, Fault Tolerant vias, generation of yield optimized cells, layout compaction, wafer mapping optimization, planarity fill, statistical timing.

References:

1. Michael Orshansky, Sani Nassif, Duane Boning, *Design for Manufacturability And StatisticalDesign: Constructive Approach*, Springer 2008
2. Chiang, Charles, Kawa, Jamil, *Design for Manufacturability and Yield for Nano-Scale CMOS*, Springer 2007
3. R S Khandpur, *Printed Circuit Boards*, Tata McGraw-Hill 2005

EC6125D DSP SYSTEM DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (10 hours)

Introduction to the course and revision on basic DSP concepts. Need for special digital signal processor. Characteristics and architectures of a typical DSP processor. Hardware multiply and accumulator, Harvard and super Harvard architecture, Architecture of SIMD, VLIW and superscalar processors. Selection of digital signal processors and benchmarking

Introduction to a popular DSP from Texas Instruments (TMS330C6000 Series - TMS320C6748), CPU Architecture - Register architecture,

Module 2: (17 hours)

TMS320C6748- CPU Data Paths and Control, Internal Data/Program Memory, on chip peripherals and interrupts, pipelining and scheduling, addressing modes, status registers, Functional units, Instruction set - fixed and floating point instructions, efficient assembly language programming. Implementation of digital signal processing algorithms in digital signal processor. C and MATLAB programming. Introduction to Code Composer Studio (CCS) IDE, The complete procedure, from creating a project in CCS to generating an executable .out file and loading it into the processor.

Module 3: (12 hours)

Introduction to VLSI DSP. Iteration bound, data flow graph representation, longest path matrix algorithm, minimum cycle mean algorithm, reduced power consumption by pipelining and parallel processing, Fast convolution algorithms, Introduction to the features of Sharc/ Tiger Sharc/ Blackfin processor series and other major vendors in the DSP market and the latest trends. FPGA based DSP system design.

References:

1. R. Chassaing*, Digital Signal Processing and Applications with the C6713 and C6416 DSK*, John Wiley and Sons, Inc., 2004
2. Welch, Thad B., Cameron HG Wright, and Michael G. Morrow*, Real-time digital signal processing from MATLAB to C with the TMS320C6x DSPs*. CRC Press, 2nd Edition, 2016.
3. On-line TI materials for the TMS320C6748:
4. Keshab K Parhi, *VLSI digital signal processing systems: design and implementation*, John Wiley & Sons,1st Edition 2007.
5. Meyer-Baese U, *Digital Signal Processing with Field Programmable Gate Arrays*, Springer, 2nd Edition, 2007.

EC6126D NETWORKING AND IoT

Pre-requisite: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1 (13 hours)

IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations. M2M and IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service(XaaS), M2M and IoT Analytics, Knowledge Management

Module 3: (13 hours)

IoT Architecture-State of the Art – Introduction, State of the art, Reference Model and architecture, IoT reference Model - IoT Reference Architecture Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints-hardware Data representation and visualization, Interaction and remote control.

Module 3 (13 hours)

IOT Data Link Layer & Network layer Protocols PHY/MAC Layer(3GPP MTC, IEEE 802.11, IEEE 802.15), ,Wireless Hart mZ-Wave,Bluetooth Low Energy, Zigbee Smart Energy, - Network Layer-IPv4, IPv6, 6LoWPAN, DHCP, ICMP, RPL, CORPL, CARP. Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, CoAP, XMPP, AMQP, MQTT-Service Layer -oneM2M, ETSI M2M, OMA, BBF – Security in IoT Protocols – MAC 802.15.4 , 6LoWPAN, RPL, Application Layer

References:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos,David Boyle,*From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence*, 1 st Edition, Academic Press, 2014.
2. Peter Waher*, Learning Internet of Things*, Packtpublishing Ltd, 2015.
3. Dieter Uckelmann, Mark Harrison, Florian Michahelles, *Architecting the Internet of Things*, Springer, 2011
4. Daniel Minoli,*Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications*, Wiley, 2013
5. Vijay Madisetti, ArshdeepBahga, *Internet of Things (A Hands-on-Approach),*Orient Blackswan Private Limited, 2015

EC6127D MECHATRONICS

Pre-requisite: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1 (14 hours)

Introduction to mechatronics. Mechatronics in manufacturing, products and design.

Mechatronic Elements- Data conversion devices, sensors, micro-sensors, transducers, signal processing devices, relays, contactors and timers.

Drives and mechanisms- Drives: stepper motors, servo drives. BLDC Motors, Ball screws, linear motion bearings, cams, systems controlled by camshafts, electronic cams, indexing mechanisms, tool magazines, and transfer systems.

Module 2 (14 hours)

Microprocessors, microcontrollers, PID controllers and PLCs.

Hydraulic systems: flow, pressure and direction control valves, actuators, and supporting elements, hydraulic power packs, and pumps. Design of hydraulic circuits.

Pneumatics: production, distribution and conditioning of compressed air, system components and graphic representations, design of systems.

Module 3 (11 hours)

Magnetic actuators,CNC machines and part programming. Industrial Robotics, Micro-Electro Mechanical Systems (MEMS).

Design examples of mechatronic systems.

References:

1. Lawrence J. Kamm, *Understanding electromechanical engineering:an introduction to mechatronics*, PHI, 2004
2. Robert H. Bishop, *Mechatronic systems, sensors, and actuators : fundamentals and modeling*, Taylor and Francis, 2008
3. HMT ltd. *Mechatronics*, Tata Mcgraw-Hill, New Delhi, 1988
4. Boucher, T. O., *Computer automation in manufacturing - an Introduction*, Chapman and Hall, 1996.

EC6128D BIOMEDICAL INSTRUMENTATION

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (12 hours)

Fundamentals of medical instrumentation – physiological systems of body –regulation of medical devices
– origin of bio potentials – Sodium –Potassium pump –Goldman Hodgkin – Katz equation – biomedical transducers – electrode-electrolyte interface – half cell potential – ECG – 12 lead systems – heart rate variability – cardiac pacemakers – defibrillators - EMG – EEG

Module 2: (16 hours)

Measurement of cardiac output – indicator dilution method – ultrasonic blood flow meter – electromagnetic blood flow meter – blood pressure measurement – oximetry – ear oximeter – pulse oximeter –skin reflectance oximeter -measurement on pulmonary system – spirometry –pulmonary function analyzers –ventilators.- Radiotherapy – Cobalt 60 machine – medical linear accelerator machine–audiometry - electrical safety in hospitals

Module 3: (11 hours)

Lasers in medicine – Argon laser – Carbon dioxide laser -laser safety –X ray applications –X-ray machine
– dental X-ray machine – ultra sound in medicine –electro therapy – hemodialysis –artificial kidney – dialyzers –membranes for hemodialysis, Measurement of pH , pCO_2 , pO_2.

References:

1. Geddes &Baker ,*Principles of applied biomedical instrumentation*, Wiley Inter science , 3rd edition,1975.
2. R S Khandpur, *Hand book of Biomedical instrumentation*, TMH,4th edition, 1987.
3. Cromwell Leslie, *Biomedical instrumentation and measurements*, PHI, 1980.
4. Brown Carr*, Introduction to Biomedical equipment technology* , Prentice Hall, 1981
5. John Enderle*, Introduction to Biomedical engineering* , Academic Press, 2005
6. Joseph D Bronzino, *Biomedical engineering hand book*, CRC Press, 2000

EC6129D ANALOG AND DATA CONVERSION SYSTEMS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (12 hours)

Sampling, Nyquist criteria, need for sample and hold circuit, sample and hold/track and hold circuits, quantization, noise in data converters, input referred noise, static non-linearity, harmonic distortion, signal-to-noise-distortion ratio, spurious free dynamic range, timing issues, aperture time and jitter, DAC architectures, binary weighted, R-2R and segmented DACs, ADC architectures, data conversion principles of flash, subranging, SAR, slope ADCs, oversampling and noise shaping ADCs

Module 2: (14 hours)

Testing of DAC, end point and linearity errors, measurement of DAC INL and DNL, oscilloscope measurements, static ADC testing using histograms (code density) with ramp input and computer-based servo loops, dynamic ADC testing using sine wave input, FFT measurements and bit error rate test, driving ADC analog inputs, gain amplifiers and level shifters using op-amps, non-ideal effects of gain amplifiers, noise in op-amps, error budget analysis of gain amplifiers, input and output errors of amplifiers, signal conditioners with auto-zero/choppers/isolation amplifiers, amplifier selection, data converter digital interfaces, driving external loads

Module 3: (13 hours)

Data converter support circuits, voltage references, low dropout voltage regulators, power supply noise reduction and filtering, analog switches and multiplexers, error sources in switches, latch up effect in CMOS switches and multiplexers, non-ideal behavior of passive resistors, capacitors and inductors, over voltage protection, ESD models and testing, Thermal design considerations for data converters, heat sink, PCB design, skin effect, transmission line, ground isolation, stray capacitance, return currents and power planes, grounding and decoupling in mixed signal systems.

References:

1. W. Kester, *The data conversion handbook*, Newnes, 2005.
2. P. Horowitz, and W. Hill, *The art of electronics*, 3rd edition, Cambridge university press, 2015.
3. W. Kester: *Mixed-signal and DSP design techniques*, Analog Devices, USA, 2000.
4. S Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, McGraw Hill, 3rdedition, 2002.
5. R. J. Baker, *CMOS- Circuit Design, Layout & Simulation*, 2nd edition, Wiley student edition, 2009.
6. Application notes of ICs.

EC6130D CONTROL SYSTEM DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1 (12 hours):
Review of basic elements of analog control systems- classical control techniques –transfer function approach- PID controller design.

State-Space Models - Controllability and state transfer - Observability and state estimation – Pole Placement– State feedback approach.

Module 2 (12 hours):

Digital control systems -Sampling and reconstruction of signals – z transforms - pulse transfer function and analysis of digital control systems - discretization methods - Cascade and feedback compensation from continuous data controllers- Dead beat controller design.

Module 3 (15hours):

Digital controllers - Root locus, Bode plot, Nyquist plot methods- Design of Digital PID controller – statespace analysis of digital control systems - Observers and their use in state-feedback loops - Observer-based controllers - -controllability and observability under discretization

Controller realization structures - canonical forms - Effects of finite word length on controllability and closed loop pole placement- Case studies

References:

1. Ogata, *Discrete time control systems*, Prentice Hall, 2013
2. Benjamin C Kuo, *Digital Control Systems*, Oxford University Press, 2005
3. Benjamin C Kuo ,Colnaraghi Farid, *Automatic Control Systems*, 8th Ed, John Wiley & Sons,2003.
4. John Dorsey, *Continuous & Discrete Control Systems*, McGrawHill, 2002.
5. John J. D'Azzo and Constantine H. Houpis, Stuart N. Sheldon, *Linear Control System Analysis and Design with MATLAB,* 5th Ed, Marcel Decker, Inc , 2003
6. Graham C Goodwin, Stefan F Graebe, Mario E Salgado*, Control System Design*, Prentice HallIndia, 2003.

EC6131D ARTIFICIAL INTELLIGENCE

Pre-requisites:Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (13 hours)

Artificial Intelligence: History and Applications, Production Systems, Structures and Strategies for state space search- Data driven and goal driven search, Depth First and Breadth First Search, DFS with Iterative Deepening, Heuristic Search- Best First Search, A* Algorithm, AO* Algorithm, Local Search Algorithms and Optimization Problems, Constraint satisfaction, Using heuristics in games- Minimax Search, Alpha Beta Procedure. Implementation of Search Algorithms in LISP.

Module 2:(13 hours)

Languages and Programming Techniques for AI- Introduction to PROLOG and LISP, Search strategies and Logic Programming in LISP, Production System examples in PROLOG

Knowledge representation - Propositional calculus, Predicate Calculus, Forward and Backward chaining, Theorem proving by Resolution, Answer Extraction, AI Representational Schemes- Semantic Nets, Conceptual Dependency, Scripts, Frames.

Module 3: (13 hours)

Introduction to Agent based problem solving. Implementation of Unification, Resolution and Answer Extraction using Resolution

Machine Learning- Symbol based and Connectionist, Social and Emergent models of learning, Planning-Planning and acting in the real World, The Genetic Algorithm- Genetic Programming, Overview of Expert System Technology- Rule based Expert Systems, Introduction to Natural Language Processing. Implementation of Machine Learning algorithms.

References:

1. George F Luger, *Artificial Intelligence- Structures and Strategies for Complex Problem Solving*, 4/e, 2002, Pearson Education.
2. E. Rich and K.Knight, *Artificial Intelligence*, 2/e, Tata McGraw Hill
3. S Russel and P Norvig, *Artificial Intelligence- A Modern Approach*, 2/e, Pearson Education, 2002
4. Nils J Nilsson, *Artificial Intelligence a new Synthesis*, Elsevier,1998
5. Ivan Bratko*, Prolog Programming for Artificial Intelligence*, 3/e, Addison Wesley, 2000
6. Dr.RussellEberhart and Dr.Yuhuishi, *Computational Intelligence - Concepts to Implementation*, Elsevier, 2007

EC6132D DATA STRUCTURES AND ALGORITHMS

Pre-requisite: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (13 hours)

General concepts of object oriented programming C++ ,Class overview-Class Definition .Access Control ,Class Scope , Constructors and Destructors , Inheritance , Polymorphism ,Overloading, Encapsulation, Friend functions, dynamic memory allocation and de-allocation. Complexity analysis, asymptotic notation, Recursion. Sorting algorithms: Selection Sort, Quick sort, Merge Sort. Abstract data types -Linked lists, Stack and Queue. Searching: Linear and Binary search implementation. Implementation of sorting, searching, linked lists, stack and queues using C++

Module 2: (13 hours)
Binary tree - in-order, pre-order and post-order traversals – representation and evaluation of arithmetic expressions using binary tree, Binary Search trees - insertion, deletion and search- Prefix, Infix and Post fix representation and conversions,-Heaps and heap sort. Implementation of tree algorithms using C++

Module 3: (13 hours)
Graph representation-Adjacency matrix, Adjacency lists- Depth First Search (DFS)-Breadth First Search(BFS),Minimum spanning tree problem - Kruskal's algorithm- Prim's algorithm Shortest path problem - Dijkstra's algorithm -Implementation of graph algorithms using C++ and the Standard Template libraryHashing -chaining –linear probing –double hashing

References:

1. D.Ravichandran ,*Programming with C++*,Third Edition,Mc Graw Hill Education, 2011
2. D.Corman, Charles E. Leiserson, Ronald L. Rivest , *Introduction to Algorithms*,Third Edition, MIT, 2009.
3. Yedidyah Langsam, MosheJ.Augenstein, AaronM.Tanenbaum, *Data Structures using C++*, Pearson Education, 2016
4. Larry Nyhoff ,ADTs,*Data Structures and Problem Solving with C++*, Second Edition, Pearson Education 2012
5. Sahni S., *Data Structures, Algorithms, and Applications in C++,* Mc Graw Hill, Singapore, 1998.

EC6133D ELECTRONIC PACKAGING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total Hours: 3

Module 1: (12 hours)

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology.

Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging.

Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference.

Module 2: (16 hours)

IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging. Different types of IC packages – DIP,QFP,etc.

Systems Packaging – MCM /SoC/SiP/SoP.

Discrete, Integrated and Embedded Passives.

Printed Circuit Board – Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards.

Board Assembly – Surface Mount Technology, Through-Hole Technology, Process Control and Design challenges.

Module 3: (11 hours)

Design for Reliability – Fundamentals, Induced failures.

Thermal Management for IC and PWBs, Cooling Requirements, Electronic cooling methods.

Electrical Testing – System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

Trends in packaging.

References:

1. Rao R. Tummala, *Fundamentals of Microsystem Packaging*McGraw Hill,2001.
2. Richard K. Ulrich &William D. Brown *Advanced Electronic Packaging* - 2nd Edition : IEEEPress, 2006
3. Rao R. Tummala, MadhavanSwaminathan, *Introduction to System-on-Package (SOP)*, McGraw-Hill, 2008.

EC6211D MOS DEVICE MODELING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (12 hours)

Energy band diagram of MOS capacitor at equilibrium – Flat band voltage – Effect of application of gate to body voltage – accumulation, depletion, weak, moderate and strong inversion conditions – non ideal insulator – threshold voltage - capacitance voltage relation – The three terminal MOS structure – effect of body bias on surface conditions – Threshold voltage with body bias.

Module 2: (12 hours)

The four terminal Metal Oxide Semiconductor transistor – strong inversion, moderate inversion and weak inversion current- voltage models – Effective mobility – Effect of source and drain series resistance – Temperature effects – Break down.

Module 3: (15 hours)

Short channel and thin oxide effects – carrier velocity saturation – channel length modulation – charge sharing – Drain Induced barrier lowering – punch through – Hot carrier effects – Impact ionization – Velocity overshoot – Ballistic operation – Quantum Mechanical effects – DC gate current – Junction leakage – Band to band tunneling - Gate Induced Drain Leakage (GIDL) – MOSFET scaling.

References:

1. Y. Tsividis& Colin McAndrew, *The MOS Transistor*, 3rd Edition, Oxford University Press, 2013.
2. NarainArora, *MOSFET modeling for VLSI simulation: Theory and Practice*, World Scientific, 2007.
3. Yuan Taur&Tak H Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2013.
4. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson, 2010
5. A.B. Bhattacharya, *Compact MOSFET Models for VLSI Design*, John Wiley, 2009

EC6213D DIGITAL VLSI TESTING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (12 hours)

Introduction to VLSI Testing process, Fault models, Fault Collapsing, Logic Simulation and Fault simulation, Combinational Circuit Test Pattern Generation - Boolean Difference, Path Sensitization Methods, D-Algorithm, PODEM, Delay fault testing, IDDQ Testing.

Module 2: (15 hours)

Combinational and Sequential SCOAP Measures, ATPG for Single-Clock Synchronous Circuits - Nine-Valued Logic and Time-Frame Expansion Methods, DFT based Sequential Circuit Testing - Adhoc design for testability - Test Point Insertion, Scan chains, Partial Scan Design, Random Access Scan, Boundary scan standard – Boundary scan cell, TAP controller, modes of operation, EXTEST, INTEST, BYPASS instructions.

Module 3: (12 hours)

Built in Self Test (BIST) - Exhaustive pattern generation, random pattern generation, LFSR for pattern generation and Output response analysis, SISR, MISR.

Memory BIST – Type of memory faults, fault detection by MARCH tests.

Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs.

References:

1. Bushnell Michael and Vishwani Agrawal, *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*, Vol. 17, Springer Science & Business Media, 2004.
2. WangLaung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI test principles and architectures: design for testability*, Academic Press, 2006.
3. AbramoviciMiron, M. A. Breuer and A. D. Friedman, *Digital Systems testing and testable design*, Computer Science Press,1990.
4. RothJr, Charles H. and Lizy K. John, *Digital systems design using VHDL*, Nelson Education, 2016.

EC6214D VLSI DIGITAL SIGNAL PROCESSING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (15 hours)

Overview of DSP Filter structures - Recursive, Non-recursive and Lattice; Performance Measures of DSP implementation - Loop bound, Iteration period, critical path, Throughput, Latency, Power; Mapping DSP Systems into Reconfigurable Logic/ASIC – Retiming, pipelining, Parallel Processing; Hardware Sharing – Unfolding and Folding.

Systolic Architecture Design – Systolic Array Design Methodology, FIR Systolic Arrays

Module 2: (12 hours)

Fast algorithms for DSP - Cook-Toom, Winograd, Iterated and Cyclic Convolution algorithms; Parallel FIR Filter structures

Finite Word Length Effects: Scaling, Round-off Noise and Coefficient Sensitivity

Low power realization of DSP algorithms, Weighted-sum computation and FIR Filters, Coefficient optimization, Circular buffer; Computational complexity and power analysis of multirate architectures, Power reduction using multirate architectures

Module 3: (12 hours)

Multiply Accumulator (MAC) - Distributed arithmetic based implementation, Techniques for Low Power Implementation of DA Based FIR Filters; Computation of Special Functions Using CORDIC

Multiplier-less implementation- Minimizing additions in weighted-sum and MCM computation, Common Sub-expression elimination, 2's Complement representation, Canonical Signed Digit (CSD) representation.

References:

1. Roger Woods, John McAllister, Ying Yi, and Gaye Lightbody, *FPGA-based implementation of signal processing systems*, John Wiley & Sons, 2008.
2. Keshab K. Parhi, *VLSI Signal Processing Systems, Design and Implementation*, John Wiley & Sons, 2008.
3. Meyer-Baese U, *Digital signal processing with field programmable gate arrays*, Springer Science & Business Media, 2007.
4. Lars Wanhammar, *DSP Integrated Circuits*, Academic Press, 1999.

EC6217D MEMS STRUCTURES AND APPLICATIONS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (12 hours)

An introduction to Micro sensors and MEMS, Classical scaling in CMOS, Moore's Law - Clean room concept, Evolution of Micro sensors & MEMS, Micro machined Micro sensors& MEMS applications: Mechanical, Inertial, Biological, Chemical, Acoustic, Integrated Smart Sensors

Module 2: (14 hours)

Microelectronic technologies for MEMS:- Oxidation:- concepts of wet and dry oxidation, Material deposition techniques:-evaporation, sputtering, CVD, PVD and MBE, Photolithography:- Positive and negative photoresists, proximity and projection lithography, Etching:- Isotropic and anisotropic etching, wet and dry etch, plasma etching, RIE etching, Micromachining :- Surface and Bulk Micromachining, general process description, problems associated to surface micromachining; LIGA process.

Module 3: (13 hours)

Microactuators:- Piezoelectric, chemical, Thermopneumatic, electrostatic and electromagnetic microactuators, MEMS Simulators and different FEA tools, Interface Electronics for MEMS, MEMS for RF Applications, Bonding & Packaging of MEMS- Direct bonding, Field assisted bonding, Bonding with an intermediate layer, General considerations in packaging design, The three levels of microsystem packaging, Packaging processing sequence, Conclusions & Future Trends.

References:

1. S. Senturia, *Microsystem Design*, Kluwer Academic Publishers, 2005.
2. Tai-ran Hsu, *MEMS and Microsystems: Design and Manufacture,* Tata McGraw-Hill.2008
3. S.K. Ghandhi, *VLSI Fabrication Principles:Silicon and Galium Arsenide*. John Wiley Inc, 2016.

EC6219D HIGH SPEED DIGITAL DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (15 hours)
Modeling of interconnects - electrical models of wires, lumped single-element models, lumped multi-element models, transmission line model, thumb rules for the applicability of models

Power supply network – local regulation with bypass capacitors, regulation with active regulators, power supply isolation

Noise sources in digital system – Noise budgeting and SNR

Module 2: (12 hours)
Signalling modes for lumped-C medium, distributed RC medium and transmission lines - simultaneous bi-directional signalling - terminations

Transmitter circuits – full swing & low swing voltage drivers, current mode drivers, Gunning transceiver logic, rise-time control

Receiver circuits – voltage & time domain performance specifications, eye diagram, static and regenerative amplifiers, integrating receivers

Module 3: (12 hours)
Timing properties of clocked storage elements, open loop timing, level sensitive clocking, pipeline timing, closed loop timing

Off-chip and on-chip clock distribution, PLL and DLL based clock aligners

Synchronisation failure and metastability, probability of synchronization failure

Hierarchy of synchronizer design – delay line, 2-register and FIFO mesochronous synchronizers

References:

1. William J Dally & John W Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998
2. Stephen H. Hall & Howard L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*, John Wiley & Sons, 2009
3. Eric Bogatin,*Signal and Power Integrity- Simplified*,2nd Edition, Prentice Hall, 2010
4. J Rabaey,*Digital Integrated Circuits: A Design Perspective*, Prentice Hall, 1996
5. Stephen H. Hall, Garrett W. Hall&James A. McCall,*High-Speed Digital System Design - A Handbook of Interconnect Theory and Design Practices*, John Wiley & Sons, 2000

EC6220D LOW POWER VLSI

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (14 hours)

Review of power dissipation in CMOS Circuits – sources of power dissipation - static, dynamic and leakage power dissipation –

Dynamic power reduction – Supply voltage scaling approaches: Optimal Transistor Sizing with Voltage Scaling, parallelism, pipelining, optimal supply voltage, using multiple supply voltage, multiple device threshold, Dynamic voltage and frequency scaling, feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization

Module 2: (13 hours)

Minimizing Switched Capacitance –Switching activity reduction, algorithmic optimization, architecture optimization, logic optimization, circuit optimization, Different logic styles – static and dynamic logic, Clock gating, reducing glitching through path balancing, input reordering

RTL Coding for low power – Glitch reduction, clock gating, gated clock FSM, precomputation, bus encoding

Module 3: (12 hours)

Leakage Reduction Techniques – Transistor stacks, power gating, Multi-Threshold CMOS, Variable-Threshold CMOS, Dynamic Threshold CMOS, Fabrication of multiple threshold voltages

Low-power CMOS Random Access Memory Circuits, Adiabatic circuits, Asynchronous system basics

References:

1. Roy Kaushik and Sharat C. Prasad, *Low-power CMOS VLSI circuit design*, John Wiley & Sons, 2009.
2. Yeap Gary K,*Practical low power digital VLSI design*, Springer Science & Business Media, 2012.
3. BellaouarAbdellatif and Mohamed Elmasry, *Low-power digital VLSI design: circuits and systems*, Springer Science & Business Media, 2012.
4. Piguet C, *Low-power CMOS circuits: technology, logic design and CAD tools*. CRC Press, 2005.
5. Jan M Rabaey, *Digital Integrated Circuits - A Design Perspective*,Prentice Hall, 2nd Edition, 2005

EC6224D VERIFICATION OF VLSI SYSTEMS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Module 1: (13 hours)

Introduction to functional verification - HDL and HVL languages - Functional verification approaches verification technologies – code coverage – functional coverage - requirements specification and the verification plan – levels of verification – directed testbench – coverage driven random based approach–Introduction to SystemVerilog - data types, arrays, structures and unions – procedural blocks, tasks and functions – procedural statements – design hierarchy – interfaces.

Module 2: (13 hours)

High level modeling – data abstraction – OOPS – parallel simulation – race condition – simple and complex stimulus and response – bus functional models – response monitors – transaction level interface– self checking testbenches – reference models – transfer function – scoreboarding – monitors -randomization in SystemVerilog – constrained random verification – random device configuration.

Module 3: (13 hours)

Functional coverage in SystemVerilog – Covergroup/Coverpoint – coverage monitoring – Verification methodology - OVM/UVM basics – System on chip verification – system level and block level verification. Introduction to formal verification – basics of equivalence checking and model checking – Boolean satisfiability (SAT) – assertion based verification – SystemVerilog assertions.

References:

1. Sutherland, Stuart, Davidmann, Simon, Flake, Peter,*SystemVerilog for Design:A Guide to Using SystemVerilog for Hardware Design and Modeling*", Second Edition, Springer Science & Business Media, 2006.
2. Chris Spear, Greg Tumbush, *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*, 3rd Edition, Springer Science & Business Media, 2012.
3. Bergeron, J.,*Writing Testbenches using SystemVerilog*, Springer, USA, 2006.
4. Rashinkar P, Paterson P, Singh L., *System-on-a-chip verification: methodology and techniques*, Springer Science & Business Media; 2007
5. Erik Seligman, Tom Schubert, M V AchuthaKiran Kumar, *Formal Verification: An Essential Toolkit for Modern VLSI Design*, Morgan Kaufmann, 2015