CURRICULUM AND SYLLABUS OF
M. TECH. DEGREE PROGRAMME IN MICROELECTRONICS & VLSI DESIGN

(Applicable from 2018 admission)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY CALICUT

DEPARTMENT OF ELECTRONICS AND

COMMUNICATION ENGINEERING

Vision of the Department

The Department of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering.

Mission of the Department

The mission of the Department of Electronics and Communication Engineering is to impart high quality technical education by offering undergraduate, graduate and research programs in the domain of Electronics and Communication Engineering with thorough foundation in theory along with strong hands-on design and laboratory components, tools and skills necessary for the students to become successful major contributors to society and profession.

Program Educational Objectives (PEOs)

PEO 1	Graduates apply their theoretical foundation and research skills in Semiconductor devices, VLSI Circuits and Systems and expertise in modern CAD and EDA tools to identify, analyze and solve engineering problems pertaining to Microelectronics and VLSI Design
PEO 2	Graduates apply their subject knowledge, communication skills and leadership qualities to build their chosen career in the area of Microelectronics and VLSI Design and allied fields.
PEO 3	Graduates exhibit ethical attitude and sensitivity to social, environmental and economic issues. in their professional activities.
PEO 4	Graduates possess a high level of motivation to continue in their chosen field of career and to acquire greater technical knowledge and develop higher skills as technology advances.

Programme Outcomes (POs) & Programme Specific Outcomes (PSOs)

PO 1	An ability to independently carry out research /investigation and development work to solve practical problems.
PO 2	An ability to write and present a substantial technical report/document.
PO 3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PSO 1	Provide strong theoretical foundation and research skills in the area of Microelectronics and VLSI Design that enable graduates to take up the challenges of the state of the art technology.
PSO 2	Encourage continuous learning in the area of Microelectronics & VLSI Design so that the graduates feel confident enough to face the challenges of the rapidly changing global scenario and come up with innovative ideas for improvement.

Curriculum for M. Tech. EC62 Microelectronics and VLSI Design

Semester 1

Sl. No	Code	Title	L	T	P	C
1	EC6201D	Digital Integrated Circuit Design	3	0	2	4
2	EC6202D	Analog Integrated Circuit Design	3	0	2	4
3	EC6203D	Advanced Semiconductor Device Modeling	3	0	2	4
4		Elective 1	3	0	0	3
5		Elective 2	3	0	0	3
		Total Credits				18

Semester 2

Sl. No	Code	Title	L	T	P	C
1	EC6204D	VLSI Technology	3	0	0	3
2	EC6205D	Physical Design Automation	3	0	2	4
4	EC6206D	Seminar	0	0	2	1
5		Elective 3	3	0	0	3
6		Elective 4	3	0	0	3
7		Elective 5	3	0	0	3
		Total Credits				17

Semester 3

Sl. No	Code	Title	L	T	P	C
1	EC7201D	Project - Part 1	0	0	24	12
		Total Credits				12

Semester 4

Sl. No.	Code	Title	L	T	P	C
1	EC7202D	Project - Part 2	0	0	26	13
		Total Credits				13

Electives

Sl. No	Code	Title	L	T	P	C
1	EC6211D	MOS Device Modeling	3	0	0	3
2	EC6212D	Analog System Design	3	0	0	3
3	EC6213D	Digital VLSI Testing	3	0	0	3
4	EC6214D	VLSI Digital Signal Processing	3	0	0	3
5	EC6215D	Compound Semiconductor Devices and applications	3	0	0	3
6	EC6216D	Power Semiconductor Devices and Technology	3	0	0	3
7	EC6217D	MEMS Structures and Applications	3	0	0	3
8	EC6218D	CMOS Image Sensors	3	0	0	3
9	EC6219D	High Speed Digital Design	3	0	0	3
10	EC6220D	Low Power VLSI	3	0	0	3
11	EC6221D	VLSI Data Converters	3	0	0	3
12	EC6222D	CMOS RF IC Design	3	0	0	3
13	EC6223D	Foundations of VLSI CAD	3	0	0	3
14	EC6224D	Verification of VLSI Systems	3	0	0	3
15	EC6225D	SOI Device Modeling and Simulation	3	0	0	3
16	EC6121D	Advanced Embedded Computing	3	0	0	3
17	EC6124D	Design for Manufacturability	3	0	0	3
18	EC6131D	Artificial Intelligence	3	0	0	3
19	EC6132D	Data Structures and Algorithms	3	0	0	3
20	EC6133D	Electronic Packaging	3	0	0	3

Notes

1. A minimum of 60 credits have to be earned for the award of M. Tech Degree in this Programme.
2. A minimum of three elective courses is to be credited from the list of electives specified for the stream with the consent of the respective faculty.
3. A maximum of two theory electives can be credited from any other specializations, offered by the institute at M. Tech. level, with the consent of the HOD, the Programme Coordinator and the Course Faculty.

EC6201D DIGITAL INTEGRATED CIRCUIT DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	2	4

Total hours: 39L + 26P

Course Outcomes:

CO1: Calculate various parameters and short channel effects of a MOSFET

CO2: Derive static and dynamic characteristics of digital CMOS circuits

CO3: Design and simulate static and dynamic CMOS logic circuits for a given functionality and speed, power consumption and area requirements

CO4: Design SRAM and DRAM cells using CMOS

Module 1: (10 hours)

Review of MOSFET threshold voltage, current, channel length modulation, body bias effect, Scaling and short channel effects, latch up effect, MOS switch, MOSFET capacitances, CMOS layout elements, parasitics, wires and vias - design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Module 2: (14 hours)

CMOS inverter, static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, Simulation of static and dynamic characteristics, layout, post layout simulation

Module 3: (15 hours)

Static CMOS design, Complementary MOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS – Course project

CMOS memory design – SRAM, DRAM and CAM memory design

References:

1. Jan M Rabaey, *Digital Integrated Circuits - A Design Perspective*, Prentice Hall, 2nd Edition, 2005
2. Sung-Mo Kang & Yusuf Leblebici, *CMOS Digital Integrated Circuits - Analysis & Design*, MGH, 3rd Edition, 2003
3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, *Analysis and Design of Digital Integrated Circuits*, 3rd Edition, McGraw-Hill, 2004
4. R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS circuit design, layout, and simulation*, Wiley-IEEE Press, 2007
5. Christopher Saint and Judy Saint, *IC layout basics: A practical guide*, McGraw-Hill Professional, 2002

EC6202D ANALOG INTEGRATED CIRCUIT DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	2	4

Total hours: 39L + 26P

Course Outcomes:

CO1: Model various components in CMOS process to estimate their performance in circuits.

CO2: Obtain the design of the biasing circuits for CMOS amplifiers.

CO3: Design single stage amplifiers and various stages of an operational amplifier.

CO4: Design fully differential amplifiers and comparators

Module 1: (10 hours)

Components available in a CMOS process; Resistors; Random and systematic mismatch; Layout techniques to minimize mismatch, Resistor model; Capacitors, MOS transistor layout; 4 terminal MOS transistor model; Threshold voltage, Drain current, Body bias effect, Channel length modulation, Influence of body effect on small and large signal behaviour of basic amplifier circuits, Small signal model of the MOS transistor; Low frequency MOSFET model, High frequency MOSFET model, Transit frequency, MOS transistor mismatch; Noise, Basics of noise-variance, autocorrelation, spectral density; Resistor noise, kT/C across a capacitor; MOS transistor noise, MOS transistor thermal and flicker noise

Module 2: (16 hours)

Current sources and sinks, Current mirrors, Matching considerations in current mirrors, Concept of current steering, Self biasing circuits, Constant Gm biasing, Start-up circuits, Bandgap referenced biasing, voltage references

Single transistor amplifiers – Telescopic Cascode amplifier, Folded cascade amplifier, Differential amplifier Noise in amplifiers, Input referred noise - Operational amplifiers - Frequency response of the amplifiers Negative feedback and stability, loop gain and unity loop gain frequency, feedback compensation, opamp offset, swing limits, slew rate, Design of single stage and multistage Operational amplifiers- Noise in operational amplifier, Effect of transistor mismatches in the performance of amplifiers

Module 3: (13 hours)

Fully differential opamps, Analysis of fully differential circuits using common-mode and differential half circuits, common mode feedback, CMFB circuits, Common mode feedback loop stability, Fully differential two stage opamp

CMOS comparator, comparator parameters: Sensitivity, Offset, speed, power dissipation, power supply rejection, input capacitance, kickback noise, Metastability, input CM range, Comparator design issues, Offset cancellation, Correlated Double sampling, Differential comparators, Latches, Pre amplifier stages.

References:

1. B.Razavi, *Design of Analog CMOS Integrated Circuit*, 2nd Edition Mc Graw Hill India, 2017
2. P. Allen & D. Holberg, *CMOS Analog Circuit Design*, 3rd Edition, Oxford University Press, 2013
3. R.J. Baker, *CMOS Circuit Design, Layout and Simulation*, 3nd Edition, Wiley-Blackwell , 2010
4. Gray, Hurst, Lewis and Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley India, 2011

EC6203D ADVANCED SEMICONDUCTOR DEVICE MODELING

Pre-requisites: Nil

L	T	P	C
3	0	2	4

Total hours: 39L + 26P

Course Outcomes:

CO1: Apply the qualitative understanding of physics of semiconductors to develop quantitative models for semiconductor phenomena relevant to the field of electronics.

CO2: Model semiconductor homo junction and characterize p-n junction diodes

CO3: Analyze metal semiconductor junctions and model Metal oxide semiconductor junctions

CO4: Interpret and Model Metal oxide semiconductor FETs.

Module 1: (15 hours)

Review of semiconductor physics – quantum foundations - Semiconductor band structure, Simplified band structure models, Carrier concentration – non equilibrium – quasi Fermi levels - drift and diffusion – mobility – generation and recombination – continuity equation

Module 2: (10 hours)

Semiconductor homo junctions – Analysis of p-n junction under equilibrium and bias – energy band diagram – diode current equation – break down of p-n junctions – Metal semiconductor junction – TCAD simulation of p-n junction diodes

Module 3: (14 hours)

Metal oxide semiconductor junction – Capacitance - voltage characteristics – threshold voltage – effect of work function difference and insulator charges

Metal Oxide Semiconductor Field effect transistors – Current–voltage characteristics – Sub threshold operation- Substrate bias effects – short channel effects and MOSFET scaling

TCAD simulation of MOS capacitor and MOSFETs.

References:

1. S.M. Sze & Kwok K. Ng, *Physics of Semiconductor Devices*, 3rd Edition, Wiley, 2007.
2. B.L. Anderson & R. L. Anderson, *Fundamentals of Semiconductor Devices*, McGraw-Hill, 2005.
3. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson 2010
4. M. S. Tyagi, *Introduction to Semiconductor Materials and Devices*, John Wiley and Sons, 2004.
5. M. K. Achuthan & K. N. Bhatt, *Fundamentals of Semiconductor Devices*, 2nd Edition, McGraw-Hill, 2009.

EC6204D VLSI TECHNOLOGY

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Outline the basics of semiconductor crystal properties.

CO2: Identify the fundamentals of IC fabrication.

CO3: Illustrate the advanced methods involved in photolithography.

CO4: Build an idea on process integration – NMOS, CMOS and Bipolar process.

Module 1: (13 hours)

Material properties, crystal structure, lattice, basis, planes, directions, angle between

different planes, phase diagram and solid solubility, Crystal growth techniques, Epitaxy, Clean room and safety requirements. Oxidation: wet and dry oxidation, Deal-Grove model, Diffusion process, Ion implantation, modeling of Ion implantation, statistics of ion implantation, rapid thermal annealing, SIMS.

Module 2: (15 hours)

Deposition & Growth: Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating, LPCVD, MBE, ALCVD, Growth of High k and low k dielectrics, Etching - wet and dry etch, plasma and RIE etch, Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, resolution, depth of focus, numerical aperture sensitivity, contrast, proximity and projection lithography, step and scan, optical proximity correction.

Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL

Module 3: (11 hours)

Planarization Techniques: Need for planarization, Chemical Mechanical Polishing

Copper damascene process; Multi-level metallization schemes, Process integration: Bipolar process, NMOS and CMOS.

References:

1. James Plummer, M. Deal and P.Griffin, *Silicon VLSI Technology*, Prentice Hall Electronics, 2010
2. S.M. Sze, Stephen Campbell, *The Science and Engineering of Microelectronics*, Oxford University Press, 2012.
3. S.K. Ghandhi, *VLSI Fabrication Principles*, John Wiley Inc, New York, 2005.

EC6205D PHYSICAL DESIGN AUTOMATION

Pre-requisites: Nil

L	T	P	C
3	0	2	4

Total hours: 39L + 26P

Course Outcomes:

CO1: Identify the issues at various stages of VLSI physical design.

CO2: Develop algorithms to solve the complex physical design problems in ICs.

CO3: Analyze and optimize the algorithms that help in the back end design of complex chips.

CO4: Apply physical design techniques and design an IC for specific area, delay and power requirements.

Module 1: (12 hours)

Introduction to digital IC design - custom and semicustom flow, combinational logic synthesis - Technology independent and technology dependent optimization - Binary decision diagrams - High level synthesis- Scheduling and allocation – Physical design – terminology – graph algorithms – heuristic algorithms – Basic Unix/Linux commands – introduction to C shell/Perl scripting.

Module 2: (13 hours)

Partitioning - Constructive and iterative algorithms - Kernighan-Lin algorithm - Fiduccia-Mattheyses algorithm - Simulated annealing and evolution – Floor planning - slicing and non-slicing floor plan - polish expression - constraint based, analytical, rectangular dual graph, hierarchical tree methods - Pin assignment – general and channel pin assignment – Placement – cost function – simulation, partitioning and performance based placement algorithms.

Module 3: (14 hours)

Routing – Global routing - maze routing, line search, Steiner tree based algorithms – Detailed routing – constraint graphs – Channel routing - left edge algorithm – dog leg routing – Switch box routing – Over the cell routing – Clock network – design considerations – clock tree synthesis - Power and ground routing - Static Timing Analysis and Timing Closure.

References:

1. Naveed A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Springer, 3rd Edition, 1999
2. Gerez, Sabih H., *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2006.
3. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, *VLSI Physical Design: from graph partitioning to timing closure*, Springer Science & Business Media, 2011.
4. Alpert, Charles J., Dinesh P. Mehta, and Sachin S. Sapatnekar, *Handbook of algorithms for physical design automation*, CRC press, 2008.
5. Sobell, Mark G., and Matthew Helmke, *A practical guide to Linux commands, editors, and shell programming*, Pearson Education India, 3rd Edition, 2013.

EC6206D SEMINAR

Pre-requisites: Nil

L	T	P	C
0	0	2	1

Total Hours: 26

Course Outcomes:

CO1: Survey the literature on new research areas and compile findings on a particular topic

CO2: Organize and illustrate technical documentation with scientific rigor and adequate literal standards on the chosen topic strictly abiding by professional ethics while reporting results and stating claims.

CO3: Demonstrate communication skills in conveying the technical documentation via oral presentations using modern presentation tools.

The objective of the seminar is to impart training to the students in collecting materials on a specific topic in the broad domain of Engineering/Science from books, journals and other sources, compressing and organizing them in a logical sequence, and presenting the matter effectively both orally and as a technical report. The topic should not be a replica of what is contained in the syllabi of various courses of the M. Tech program. The topic chosen by the student shall be approved by the Faculty-in-Charge of the seminar. The seminar evaluation committee shall evaluate the presentation of students. A seminar report duly certified by the Faculty-in-Charge of the seminar in the prescribed form shall be submitted to the department after the approval from the committee.

EC7201D PROJECT: PART 1

Pre-requisites : Nil

L	T	P	C
0	0	24	12

Total Hours: 312

Course Outcomes:

CO1: Develop aptitude for research and independent learning.

CO2: Demonstrate the ability to carry out literature survey and select unresolved problems in the domain of the selected project topic.

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4: Acquire the knowledge and awareness to carry out cost-effective and environment friendly designs.

CO5: Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals.

The major project in the third and fourth semesters offer the opportunity to apply and extend knowledge acquired in the first year of the M. Tech. program. The major project can be analytical work, simulation, hardware design or a combination of these in the emerging areas of Microelectronics and VLSI Design under the supervision of a faculty from the ECE Department. The specific project topic undertaken will reflect the common interests and expertise of the student(s) and supervisor. Students will be required to 1) perform a literature search to review current knowledge and developments in the chosen technical area; 2) undertake detailed technical work in the chosen area using one or more of the following:

- Analytical models
- Computer simulations
- Hardware implementation

The emphasis of major project shall be on facilitating student learning in technical, project management and presentation spheres. Project work will be carried out individually. The M. Tech. project evaluation committee of the department shall evaluate the project work during the third semester in two phases. The first evaluation shall be conducted in the middle of the semester. This should be followed by the end semester evaluation. By the time of the first evaluation, students are expected to complete the literature review, have a clear idea of the work to be done, and have learnt the analytical / software / hardware tools. By the time of the second evaluation, they are expected to present the results of their advancements in the chosen topic, write an interim technical report of the study and results and clearly state the work plan for the next semester.

EC7202D PROJECT: PART 2

Pre-requisites: Successful completion of EC7201D Project: Part 1

L	T	P	C
0	0	26	13

Total Hours: 338

Course Outcomes:

CO1: Develop aptitude for research and independent learning.

CO2: Demonstrate the ability to carry out literature survey and select unresolved problems in the domain of the selected project topic.

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4: Acquire the knowledge and awareness to carry out cost-effective and environment friendly designs.

CO5: Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals.

EC7202D Project: Part 2 is a continuation of EC7201D Project: Part 1in the third semester. Students should complete the work planned in the third semester, attaining all the objectives, and should prepare the project report of the complete work done in the two semesters. They are expected to communicate their innovative ideas and results in reputed conferences and/or journals. The M. Tech. project evaluation committee of the department shall evaluate the project work during the fourth semester in two phases. The first evaluation shall be conducted towards the end of the semester. This should be followed by a second evaluation by the committee including an external examiner.

EC6211D MOS DEVICE MODELING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Apply the qualitative understanding of Metal oxide Semiconductor system to derive quantitative models for potential -charge relation and capacitance effects.

CO2: Model the body bias effects on the operation of an MOS system.

CO3: Analyze the physics of four terminal MOS system and interpret the current voltage relation of a Metal oxide semiconductor field effect transistor.

CO4: Model the small channel and thin oxide effects in MOSFET operation.

Module 1: (12 hours)

Energy band diagram of MOS capacitor at equilibrium – Flat band voltage – Effect of application of gate to body voltage – accumulation, depletion, weak, moderate and strong inversion conditions – non ideal insulator – threshold voltage - capacitance voltage relation – The three terminal MOS structure – effect of body bias on surface conditions – Threshold voltage with body bias

Module 2: (12 hours)

The four terminal Metal Oxide Semiconductor transistor – strong inversion, moderate inversion and weak inversion current - voltage models – Effective mobility – Effect of source and drain series resistance – Temperature effects – Break down

Module 3: (15 hours)

Short channel and thin oxide effects – carrier velocity saturation – channel length modulation – charge sharing – Drain Induced barrier lowering – punch through – Hot carrier effects – Impact ionization – Velocity overshoot – Ballistic operation – Quantum Mechanical effects – DC gate current – Junction leakage – Band to band tunneling - Gate Induced Drain Leakage (GIDL) – MOSFET scaling

References:

1. Y. Tsividis & Colin McAndrew, *The MOS Transistor*, 3rd Edition, Oxford University Press, 2013.
2. Narain Arora, *MOSFET modeling for VLSI simulation: Theory and Practice*, World Scientific, 2007.
3. Yuan Taur & Tak H Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2013.
4. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson, 2010
5. A. B. Bhattacharya, *Compact MOSFET Models for VLSI Design*, John Wiley, 2009

EC6212D ANALOG SYSTEM DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Design op-amps for applications demanding high speed, low power and rail-to-rail swing

CO2: Make use of the knowledge on continuous time filters to realize discrete switched capacitor filters

CO3: Analyze simple and charge pump PLLs using linear models

CO4: Design sub blocks to meet the specifications of a PLL

Module 1: (12 hours)

Frequency compensation in feedback amplifiers, review of Miller compensation, feed forward topologies, Gain boosting in amplifiers, low power and low noise, low offset op-amps, high slew rate and fast settling op-amps, constant g_m rail-to-rail input stage op-amps, output power efficiency, class AB biasing, output saturation protection and current limiting, analog circuit layout, op amp design using a SPICE tool

Module 2: (11 hours)

Resistor emulation using a MOSFET and capacitor, charge injection, clock feed-through, switched capacitor integrators, non-overlapping clock, switched capacitor gain circuits, first order and second order filters, switch sharing, low-Q and high-Q biquad filters, op-amps for switched capacitor circuits, Gm-C filters, CMOS transconductors, active RC and MOSFET-C filters, frequency and Q-factor tuning.

Module 3: (16 hours)

Operating principle of PLL, phase detector, XOR, JK FF and phase frequency detector, first order loop filters, voltage controlled oscillators, ring and LC oscillators, tuning range of VCOs, first order PLL, locked condition, transient response of PLL in the locked state, charge pump PLL, PFD/CP non-idealities, loop filter design, stability of the loop, fast lock technique, jitter in PLL, sources of noise in PLL, phase noise in PLL.

References:

1. J. Huijsing, *Operational amplifiers Theory and design*, 3rd Edition, Springer, 2017.
2. P. Allen and D. Holberg, *CMOS Analog Circuit Design*, 3rd Edition, Oxford University Press, 2013
3. R. Gregorian and G. C. Temes, *Analog MOS integrated circuits for signal processing*, Wiley India Pvt Limited, 1986.
4. T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd Edition, John Wiley & Sons, USA. 2012.
5. R. E. Best, *Phase-locked loops, design, simulation and applications*, 6th Edition, McGraw-Hill professional, 2007.

EC6213D DIGITAL VLSI TESTING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Develop test patterns required to detect faults in a circuit

CO2: Determine the testability of a circuit

CO3: Design methods/techniques to improve the testability of digital circuits.

CO4: Design Logic BIST circuits based on LFSRs

Module 1: (12 hours)

Introduction to VLSI Testing process, Fault models, Fault Collapsing, Logic Simulation and Fault simulation, Combinational Circuit Test Pattern Generation - Boolean Difference, Path Sensitization Methods, D-Algorithm, PODEM, Delay fault testing, IDDQ Testing

Module 2: (15 hours)

Combinational and Sequential SCOAP Measures, ATPG for Single-Clock Synchronous Circuits - Nine-Valued Logic and Time-Frame Expansion Methods, DFT based Sequential Circuit Testing - Adhoc design for testability - Test Point Insertion, Scan chains, Partial Scan Design, Random Access Scan, Boundary scan standard – Boundary scan cell, TAP controller, modes of operation, EXTEST, INTEST, BYPASS instructions

Module 3: (12 hours)

Built in Self-Test (BIST) - Exhaustive pattern generation, random pattern generation, LFSR for pattern generation and Output response analysis, SISR, MISR

Memory BIST – Type of memory faults, fault detection by MARCH tests

Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs

References:

1. Bushnell Michael and Vishwani Agrawal, *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*, Vol. 17, Springer Science & Business Media, 2004.
2. Wang Laung-Terng, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI test principles and architectures: design for testability*, Academic Press, 2006.
3. Abramovici Miron, M. A. Breuer and A. D. Friedman, *Digital Systems testing and testable design*, Computer Science Press, 1990.
4. Roth Jr, Charles H. and Lizy K. John, *Digital systems design using VHDL*, Nelson Education, 2016.

EC6214D VLSI DIGITAL SIGNAL PROCESSING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Identify the performance parameters of DSP implementation for hardware mapping

CO2: Apply different techniques to map DSP systems into reconfigurable logic/ASIC

CO3: Utilize the methods for the low power implementation of DSP algorithms

CO4: Design and implement multiplier-less DSP systems

Module 1: (15 hours)

Overview of DSP Filter structures - Recursive, Non-recursive and Lattice; Performance Measures of DSP implementation - Loop bound, Iteration period, critical path, Throughput, Latency, Power; Mapping DSP Systems into Reconfigurable Logic/ASIC – Retiming, pipelining, Parallel Processing; Hardware Sharing – Unfolding and Folding

Systolic Architecture Design – Systolic Array Design Methodology, FIR Systolic Arrays

Module 2: (12 hours)

Fast algorithms for DSP - Cook-Toom, Winograd, Iterated and Cyclic Convolution algorithms; Parallel FIR Filter structures

Finite Word Length Effects: Scaling, Round-off Noise and Coefficient Sensitivity

Low power realization of DSP algorithms, Weighted-sum computation and FIR Filters, Coefficient optimization, Circular buffer; Computational complexity and power analysis of multirate architectures, Power reduction using multirate architectures

Module 3: (12 hours)

Multiply Accumulator (MAC) - Distributed arithmetic based implementation, Techniques for Low Power Implementation of DA Based FIR Filters; Computation of Special Functions Using CORDIC

Multiplier-less implementation- Minimizing additions in weighted-sum and MCM computation, Common Sub-expression elimination, 2's Complement representation, Canonical Signed Digit (CSD) representation.

References:

1. Roger Woods, John McAllister, Ying Yi, and Gaye Lightbody, *FPGA-based implementation of signal processing systems*, John Wiley & Sons, 2008.
2. Keshab K. Parhi, *VLSI Signal Processing Systems, Design and Implementation*, John Wiley & Sons, 2008.
3. Meyer-Baese U, *Digital signal processing with field programmable gate arrays*, Springer Science & Business Media, 2007.
4. Lars Wanhammar, *DSP Integrated Circuits*, Academic Press, 1999.

EC6215D COMPOUND SEMICONDUCTOR DEVICES AND APPLICATIONS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Interpret important parameters governing the high speed performance of devices and circuits

CO2: Model the properties of Hetero junctions from the energy band diagram point of view

CO3: Model the Physics and operation and modeling of MESFETs

CO4: Interpret the operation and modeling of Hetero junction Bipolar Transistor

Module 1: (13 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature - Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices - Band diagrams, homo and hetero junctions

Module 2: (13 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current.

Module 3: (13 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET (MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices

References:

1. B. J. Baliga, Gallium Nitride and Silicon Carbide Power Devices, World Scientific, 2017.
2. Sandip Tiwari, *Compound Semiconductor Device Physics*, Academic Press, 1992.
3. Ruediger Quay, *Gallium Nitride Electronics*, Springer 2008.
4. S. M. Sze, *High-Speed Semiconductor Devices*, Wiley, 1990.
5. Avishay Katz, *Indium Phosphide and Related materials: Processing, Technology and Devices*, Artech House, 1992
6. Ralph E. Williams, *Modern GaAs Processing Methods*, Artech House, 1990

EC6216D POWER SEMICONDUCTORS DEVICES AND TECHNOLOGY

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Interpret the physics of avalanche break down mechanism in power diodes

CO2: Model the applications of power BJT as a switch and explore typical switching applications

CO3: Explain Silicon power MOSFET theory and its applications

CO4: Model the operation of Silicon Carbide power MOSFET theory and its applications

Module 1: (10 hours)

Silicon power diodes - Avalanche Breakdown voltage of Silicon planar p-n junctions, Breakdown voltage improvement Techniques – Floating field rings – field plates - MESA structures.

High injection level effects in pn junctions. Forward voltage drop in high voltage PIN diodes - independence on carrier lifetime.

Module 2: (13 hours)

Silicon Bipolar Power Transistor structures and characteristics, Current-gain, Switching operation, second break down and safe operating area.

Silicon Power MOSFETs, I-V characteristics, on resistance, Minimum size chip design for specific drain breakdown voltage, Switching characteristics, Safe operating area, Insulated Gate Bipolar Transistor (IGBT) – Structure, Operation principle, I-V characteristics and turn off transients, Latch up and its prevention.

Module 3: (16 hours)

Silicon Carbide power Devices – Advantages of Silicon Carbide over Silicon from high power point of view – SiC Diodes – Avalanche Breakdown Voltage – SiC Power MOSFETs – Different SiC power MOSFET architectures – on state I-V characteristics – Break down voltage improvement - SiC IGBT

References:

1. Baliga, B. Jayant, Power Semiconductor Devices, PWS Publishing Co., Boston, 1996.
2. Benda, Vitezslav, John Gowar, and Duncan A. Grant, Chichester , Power semiconductor devices: theory and applications, New York Wiley, 1999.
3. B. J. Baliga., Silicon Carbide Power Devices, World Scientific, 2006.
4. B. J. Baliga, Gallium Nitride and Silicon Carbide Power Devices, World Scientific, 2017.
5. HongyuYu, TianliDuan, Gallium Nitride Power Devices, Pan Stanford 1e, 2017.

EC6217D MEMS STRUCTURES AND APPLICATIONS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Interpret the basic principle of micro sensors and actuators.

CO2: Demonstrate the basics of different micro machining technologies.

CO3: Develop knowledge on virtual fabrication based on different MEMS Simulators and different FEA tools

CO4: Analyze various bonding and packaging techniques in MEMS.

Module 1: (12 hours)

An introduction to Micro sensors and MEMS, Classical scaling in CMOS, Moore's Law - Clean room concept, Evolution of Micro sensors & MEMS, Micro machined Micro sensors& MEMS applications: Mechanical, Inertial, Biological, Chemical, Acoustic, Integrated Smart Sensors

Module 2: (14 hours)

Microelectronic technologies for MEMS:- Oxidation:- concepts of wet and dry oxidation, Material deposition techniques:-evaporation, sputtering, CVD, PVD and MBE, Photolithography:- Positive and negative photoresists, proximity and projection lithography, Etching:- Isotropic and anisotropic etching, wet and dry etch, plasma etching, RIE etching, Micromachining :- Surface and Bulk Micromachining, general process description, problems associated to surface micromachining; LIGA process.

Module 3: (13 hours)

Microactuators:- Piezoelectric, chemical, Thermopneumatic, electrostatic and electromagnetic microactuators, MEMS Simulators and different FEA tools, Interface Electronics for MEMS, MEMS for RF Applications, Bonding & Packaging of MEMS- Direct bonding, Field assisted bonding, Bonding with an intermediate layer, General considerations in packaging design, The three levels of microsystem packaging, Packaging processing sequence, Conclusions & Future Trends.

References:

1. S. Senturia, *Microsystem Design*, Kluwer Academic Publishers, 2005.
2. Tai-ran Hsu, *MEMS and Microsystems: Design and Manufacture*, Tata McGraw-Hill.2008
3. S.K. Ghandhi, *VLSI Fabrication Principles:Silicon and Galium Arsenide*. John Wiley Inc, 2016.

EC6218D CMOS IMAGE SENSORS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Compare the performance of various pixels and choose suitable architecture for an application

CO2: Distinguish various noise sources in image sensors and estimate the noise of a signal path

CO3: Design building blocks of an image sensor readout

CO4: Develop architecture-dependent design optimizations in the readout of an image sensor

Module 1: (13 hours)

Review of MOS capacitor and MOSFET, charge transfer and charge coupled systems, floating diffusion nodes, effect of thermal, shot and trap-induced noises, limitation of CCDs, photo-generated charges, photodiode, photo current, photodiodes in a standard CMOS technology, readout architectures in CMOS technology, pixel circuits, passive and 3-T active pixels, fill factor, full well capacity, sensitivity, signal dependent non-idealities, reset, temporal and photon shot noise, signal-to-noise ratio, dynamic range, imager specifications from photon transfer curve

Module 2: (11 hours)

Readout architectures, pixel, column and chip level readouts, readout dependent fixed pattern noise, double sampling techniques, correlated double sampling, pinned-photodiode, 4-T active pixel, dark current and fixed pattern noise reduction, analog, digital and mixed mode CDS, column amplifier and sensitivity, adaptive gain column amplifiers, column fixed pattern noise reduction, the impact of transfer gate on full well capacity, high dynamic range pixels, logarithmic, linear-log pixel circuits, current mode and CTIA pixels, time mode pixels

Module 3: (15 hours)

Analog-to-digital converters in pixel, column and chip level operations, pixel pitch and speed of ADCs, comparators for ADCs, slope ADCs and accelerated-ramp slope ADCs, digital and continuous ramp generators, cyclic ADC, digital error correction, multi-step data converters, column shared architectures, technology scaling on pixels, pixel pitch reduction and the performance of ADCs, amplifier reusing and scaling of capacitors in cyclic ADCs, multiple sampling and noise canceling cyclic ADCs, SAR ADCs, pixel level ADCs, applications of CMOS image sensors, characterization of an image sensor

References:

1. J. Nakamura, *Image Sensors and Signal Processing for Digital Still Cameras*, CRC Press, 2005
2. A. Theuwissen, *Solid-State Imaging with Charge-Coupled Devices*, Kluwer academic publishers, 1995.
3. M. Sarkar and A. Theuwissen, *A Biologically Inspired CMOS Image Sensor*, Springer Verlag, 2013.
4. J. R. Janesick, *Photon Transfer DN*, SPIE press, USA, 2007.
5. T. Kuroda, *Essential Principles of Image Sensors*, CRC Press, 2014.
6. Research articles from IEEE Journal of Solid State Circuits and IEEE Transactions on Electron Devices.

EC6219D HIGH SPEED DIGITAL DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Adapt to venture deep into the realm of high speed digital design

CO2: Relate to the inventory of wire models, noise, signaling and synchronization concepts associated with high speed design

CO3: Demonstrate an understanding of the concepts, thumb rules and design of basic high speed systems

CO4: Apply the understanding to the design of high speed systems and other allied fields appreciating the trade-offs between noise immunity, power, speed etc.

Module 1: (15 hours)

Modeling of interconnects - electrical models of wires, lumped single-element models, lumped multi-element models, transmission line model, thumb rules for the applicability of models

Power supply network – local regulation with bypass capacitors, regulation with active regulators, power supply isolation

Noise sources in digital system – Noise budgeting and SNR

Module 2: (12 hours)

Signalling modes for lumped-C medium, distributed RC medium and transmission lines - simultaneous bi-directional signalling - terminations

Transmitter circuits – full swing & low swing voltage drivers, current mode drivers, Gunning transceiver logic, rise-time control

Receiver circuits – voltage & time domain performance specifications, eye diagram, static and regenerative amplifiers, integrating receivers

Module 3: (12 hours)

Timing properties of clocked storage elements, open loop timing, level sensitive clocking, pipeline timing, closed loop timing

Off-chip and on-chip clock distribution, PLL and DLL based clock aligners

Synchronisation failure and metastability, probability of synchronization failure

Hierarchy of synchronizer design – delay line, 2-register and FIFO mesochronous synchronizers

References:

1. William J Dally & John W Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998
2. Stephen H. Hall & Howard L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*, John Wiley & Sons, 2009
3. Eric Bogatin, *Signal and Power Integrity- Simplified*, 2nd Edition, Prentice Hall, 2010
4. J Rabaey, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, 1996
5. Stephen H. Hall, Garrett W. Hall & James A. McCall, *High-Speed Digital System Design - A Handbook of Interconnect Theory and Design Practices*, John Wiley & Sons, 2000

EC6220D LOW POWER VLSI

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Design CMOS circuits to reduce dynamic power dissipation

CO2: Identify different methods to reduce leakage power consumption in submicron technologies

CO3: Design low power random access memories and arithmetic circuits

Module 1: (14 hours)

Review of power dissipation in CMOS Circuits – sources of power dissipation - static, dynamic and leakage power dissipation -

Dynamic power reduction – Supply voltage scaling approaches: Optimal Transistor Sizing with Voltage Scaling, parallelism, pipelining, optimal supply voltage, using multiple supply voltage, multiple device threshold, Dynamic voltage and frequency scaling, feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization

Module 2: (13 hours)

Minimizing Switched Capacitance – Switching activity reduction, algorithmic optimization, architecture optimization, logic optimization, circuit optimization, Different logic styles – static and dynamic logic, Clock gating, reducing glitching through path balancing, input reordering

RTL Coding for low power – Glitch reduction, clock gating, gated clock FSM, precomputation, bus encoding

Module 3: (12 hours)

Leakage Reduction Techniques – Transistor stacks, power gating, Multi-Threshold CMOS, Variable-Threshold CMOS, Dynamic Threshold CMOS, Fabrication of multiple threshold voltages

Low-power CMOS Random Access Memory Circuits, Adiabatic circuits, Asynchronous system basics

References:

1. Roy Kaushik and Sharat C. Prasad, *Low-power CMOS VLSI circuit design*, John Wiley & Sons, 2009.
2. Yeap Gary K, *Practical low power digital VLSI design*, Springer Science & Business Media, 2012.
3. Bellaouar Abdellatif and Mohamed Elmasry, *Low-power digital VLSI design: circuits and systems*, Springer Science & Business Media, 2012.
4. Piguet C, *Low-power CMOS circuits: technology, logic design and CAD tools*. CRC Press, 2005.
5. Jan M Rabaey, *Digital Integrated Circuits - A Design Perspective*, Prentice Hall, 2nd Edition, 2005

EC6221D VLSI DATA CONVERTERS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Compare data converters' performance based on static and dynamic specifications

CO2: Design current steering DAC with suitable segmentation

CO3: Decide the Nyquist ADC architecture and develop the architecture that meets the performance specifications

CO4: Analyze oversampling Delta-Sigma ADCs with suitable models

Module 1: (10 hours)

Sampling, Non idealities in sampling, noise and distortion in sampling, sample and hold circuits, timing issues in sample and hold circuit, bootstrapping systems, charge injection and noise, introduction to switched capacitor circuits, switched capacitor sample and hold circuits, static specifications of data converters, accuracy, nonlinearity, offset, dynamic specifications, SNR, SFDR, ENOB, dynamic range

Module 2: (16 hours)

Digital-to-analog converter in voltage, current steering DAC, segmentation, static and dynamic errors, accuracy, calibration, dynamic element matching, decoders and matrix DAC architecture design, Flash ADC, impacts of latch meta-stability, kick-back noise and offset, sub ranging and pipeline converter architectures, 1.5 bit/stage and error correction, folding and interleaving architectures, SAR ADC

Module 3: (13 hours)

Oversampling and quantization noise spectrum, linearity with oversampling, first order noise shaping, delta sigma modulator with noise shaping, switched capacitor implementation, linearized analysis, stability of delta sigma modulators, decimation filters with accumulate and dump, averaging without decimation, aliasing, interpolation filters for DAC, second order noise shaping, linearity, idle tones and dithering, multi stage noise shaping architectures, error-feedback structures

References:

1. R. J. Baker, *CMOS Mixed-Signal Circuit Design*, Wiley India Edition, 2009.
2. R. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd Edition, Springer, 2007.
3. S. Pavan, R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 2nd Edition, John Wiley & Sons, 2017.
4. M. J. M. Pelgrom, *Analog-to-Digital Conversion*, Springer, 2010.
5. T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd Edition, John Wiley & Sons, USA. 2012.

EC6222D CMOS RF IC DESIGN

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Adapt to venture deep into the RF spectrum

CO2: Relate to the inventory of RF device models

CO3: Demonstrate an understanding of the language, basic operation and design of basic RF modules

CO4: Apply the understanding to the design of wireless systems and other allied fields appreciating the trade-offs between noise, linearity, spectral cost etc.

Module 1: (13 hours)

Basics of RF circuit design - Noise: Available noise power, noise figure

Linearity & distortion: Third-order intercept point, second-order intercept point, 1-dB compression point, broadband measures of linearity - Modeling of active & passive components at high frequencies

Impedance matching: broadband matching, power matching & noise matching

High frequency amplifiers: bandwidth estimation using open-circuit & short-circuit time constants - using zeros to enhance bandwidth - shunt-series amplifiers, tuned amplifiers & cascaded amplifiers

Module 2: (13 hours)

RF power amplifiers: Design of class A, AB, B, C, D, E, F, G & H amplifiers - Low-noise amplifier (LNA).

CS, CG & cascode amplifiers, shunt-series feedback amplifiers, noise & linearity of amplifiers, amplifiers using differential configurations, Low voltage topologies for LNA, DC bias networks for LNA, design of broadband LNA

Mixers: Mixing operation, mixing with nonlinearity, mixer noise & linearity, mixer with local oscillator switching, popular mixer configurations like the Moore mixer, mixer with simultaneous noise and power match, mixer employing current reuse for low power applications

Module 3: (13 hours)

Oscillators: Negative resistance-based LC resonator, Colpitts oscillator, differential topologies, phase noise in oscillators, tunable oscillators

Phase-locked loops (PLL) & frequency synthesizers, PLL components, continuous-time and transient behavior of PLL, in-band and out-of-band phase noise

Frequency synthesizers: Integer-N & fractional-N synthesizers, spurious components in synthesizers

References:

1. John W M Rogers & Calvin Plett, *Radio Frequency Integrated Circuit Design*, 2nd Edition, Artech House, 2010
2. Richard Chi-Hsi Li, *RF Circuit Design*, John Wiley & Sons, 2009
3. Hooman Darabi, *Radio Frequency Integrated Circuits & Systems*, Cambridge University Press, 2015
4. Behzad Razavi, *RF Microelectronics*, 2nd Edition, Prentice Hall, 2012
5. Thomas H Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Edition, Cambridge University Press, 2004.

EC6223D FOUNDATIONS OF VLSI CAD

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Identify the issues at various stages of IC design.

CO2: Develop algorithms to solve the complex design problems in ICs.

CO3: Optimize the algorithms so that it can handle the design of IC containing multi million transistors.

CO4: Demonstrate capability for CAD tool development and enhancement.

Module 1: (11 hours)

Matrices - Linear dependence of vectors, solution of linear equations, bases of vector spaces, orthogonality, complementary orthogonal spaces and solution spaces of linear equations.

Module 2: (13 hours)

Graphs - representation of graphs using matrices; Paths, connectedness; circuits, cutsets, trees; Fundamental circuit and cutset matrices; Voltage and current spaces of a directed graph and their complementary orthogonality.

Module 3: (15 hours)

Algorithms and data structures: efficient representation of graphs; Elementary graph algorithms involving BFS and DFS trees, such as finding connected and 2-connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph - data structures such as stacks, linked lists and queues, binary trees and heaps - time and space complexity of algorithms - Algorithms for VLSI Physical Design - Synthesis, Circuit Simulation and Digital Design Automation.

References:

1. K. Hoffman and R. E. Kunze, *Linear Algebra*, 2nd Edition, Pearson India, 2015
2. T. Cormen, C. Leiserson and R. L. Rivest, C.Stein, *Introduction to Algorithms*, 3rd Edition, MIT Press, 2009.
3. Gerez, Sabih H., *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2006.
4. N. Balabanian and T. A. Bickart, *Linear Network Theory; Analysis, Properties, Design and Synthesis*, Matrix Publishers, Inc., 1981.
5. N. Shervani, *Algorithms for VLSI Physical Design Automation*, 3rd Edition, Kluwer Academic Publishers, 1998
6. Neil H. E. Weste and David Harris, *Principles of CMOS VLSI Design*, 3rd Edition, Addison Wesley, 2004.

EC6224D VERIFICATION OF VLSI SYSTEMS

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Estimate the effort required for verification and formulate a verification plan for complex IC designs.

CO2: Develop HVL based self-checking test benches both directed and random.

CO3: Apply techniques to assess the verification efficiency and identify the methods to improve it.

CO4: Select suitable formal verification methods for exhaustive verification of a design.

Module 1: (13 hours)

Introduction to functional verification - HDL and HVL languages - Functional verification approaches verification technologies – code coverage – functional coverage - requirements specification and the verification plan – levels of verification – directed testbench – coverage driven random based approach – Introduction to SystemVerilog - data types, arrays, structures and unions – procedural blocks, tasks and functions – procedural statements – design hierarchy – interfaces.

Module 2: (13 hours)

High level modeling – data abstraction – OOPS – parallel simulation – race condition – simple and complex stimulus and response – bus functional models – response monitors – transaction level interface – self checking testbenches – reference models – transfer function – scoreboarding – monitors - randomization in SystemVerilog – constrained random verification – random device configuration.

Module 3: (13 hours)

Functional coverage in SystemVerilog – Covergroup/Coverpoint – coverage monitoring – Verification methodology - OVM/UVM basics – System on chip verification – system level and block level verification. Introduction to formal verification – basics of equivalence checking and model checking – Boolean satisfiability (SAT) – assertion based verification – SystemVerilog assertions.

References:

1. Sutherland, Stuart, Davidmann, Simon, Flake, Peter, *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*", Second Edition, Springer Science & Business Media, 2006.
2. Chris Spear, Greg Tumbush, *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*, 3rd Edition, Springer Science & Business Media, 2012.
3. Bergeron, J., *Writing Testbenches using SystemVerilog*, Springer, USA, 2006.
4. Rashinkar P, Paterson P, Singh L., *System-on-a-chip verification: methodology and techniques*, Springer Science & Business Media; 2007
5. Erik Seligman, Tom Schubert,M V Achutha Kiran Kumar, *Formal Verification: An Essential Toolkit for Modern VLSI Design*, Morgan Kaufmann, 2015

EC6225D SOI DEVICE MODELING AND SIMULATION

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Develop and understanding of Silicon on Insulator Technology and different types of SOI MOSFET structures.

CO2: Investigate into various Technology aspects of Multiple Gate MOSFET Design.

CO3: Model the physics of Multiple Gate MOSFETs.

Module 1: (13 hours)

Silicon on insulator concept – partially depleted and fully depleted SOI MOSFETs – Advantages of SOI MOSFETs over bulk MOSFET – Single Gate, Double Gate, Triple Gate and surrounding gate SOI MOSFETs – Physics of multi gate SOI MOSFETs

Module 2: (13 hours)

Multiple Gate MOSFET Technology – Fin Design – Design of - Gate stack – source Drain Series Resistance and Capacitance – Mobility and strain Engineering – Contact to the Fins

Module 3: (13 hours)

Modeling of Multi Gate MOSFETs – Quantum Mechanical Effects – Short Channel Effects – Double Gate MOS system – Gate Voltage Effect – Semiconductor Thickness Effect – Asymmetry Effects – Oxide Thickness Effect – Electron Tunnel Current – 2 Dimensional confinement

References:

1. J. P. Colinge, *FinFETs and Other Multi-Gate Transistors*, Springer, 2007.
2. B. L. Anderson & R. L. Anderson, *Fundamentals of Semiconductor Devices*, McGraw-Hill, 2005.
3. C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson 2010.
4. Nandita Dasgupta, Amitava Dasgupta, *Semiconductor Devices: Modelling And Technology*, PHI Learning Pvt. Ltd., 2004

EC6121D ADVANCED EMBEDDED COMPUTING

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Identify the advanced architectural features of advanced Intel and ARM processors

CO2: Review and research the state of the art in internet protocols

CO3: Discuss and identify the latest short range, low power protocols

CO4: Estimate the relevance of the Linux OS and device drivers based on Linux

Module 1: (16 hours)

Architecture of Intel processors from 80286 to Pentium-Microarchitectural techniques of advanced processors –pipelining-superscalar concept –Out of order execution –Speculative execution – branch prediction –register renaming -Multicore processors- Processors beyond Pentium- Architecture of ARM Cortex-M – NVIC – WIC--Sleep modes – peripheral programming of a Cortex-M processor. Robotics – Designing robotics applications using ARM cortex-M in MSP 432 Robotics kitGPU Processing

Module 2: (13 hours)

M2M to IoT – A Market Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT. **M2M to IoT-An Architectural Overview**– Building an architecture, Main design principles and needed. An IoT architecture outline, standards considerations.Review of internet protocols –Processing platforms for IoT-sensors –actuators-Cloud computing models –low power ,low range protocols –Zigbee –BLE – 6LoWPAN. Applications for IoT-Smart home, city ,agricultureetc, - IoT services Project work on Design and development of an IoT product .

Module 3: (10 hours)

Linux and linux device drivers –Linux Internals-Project work on porting a real time OS onto an Embedded board

References:

1. Lyla B. Das, *The x86 Microprocessors: 8086 to Pentium, Multicores, Atom, and the 8051 Microcontroller: Architecture, Programming and Interfacing*, Second Edition, Pearson Education, India 2014
2. Lyla B. Das: *Architecture, Programming, and Interfacing of Low-power Processors – ARM7*, *Cortex-M*, Cengage, 2017
3. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, *From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence*, 1st Edition, Academic Press, 2014.
4. Arshdeep Bagha, Vijay Madisetti, *Internet of Things*, A hands on approach, 2015
5. Daniel P. Bovet, Marco Cesati, *Understanding the Linux Kernel*, 3rd Edition, O'Reilly, 2005

EC6124D DESIGN FOR MANUFACTURABILITY

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Appraise the product manufacturing process, importance of manufacturer, different DFM rules and guidelines.

CO2: Summarize different types of PCBs and their design considerations for manufacturability.

CO3: Analyze the manufacturability of Integrated Circuits with various design constrains.

Module 1 (15 Hours): Product Life cycle – Introduction, Growth, Mature and Saturation, Product life cycle management, What is DFM, Need of DFM – Higher Quality, Lower Cost, Faster Time to market, better Yield etc. Designer vs manufacturer.

Need for different DFM techniques for different companies – Different applications, Different manufactures, Different equipment and processes. Development of DFM rules, Design Guidelines, exceptions.

Simple assembly process vs complex and expensive components, Simple component manufacture vs complex manufacturing process, Simple and inexpensive design vs expensive and complex service and support.

DFM softwares. Emerging manufacturing trends, Lead free design, standard design processes, Certifications. Over view of Design for Testability, Design for Assembly, Design for serviceability, Design for reliability etc.

Module 2 (14 Hours):PCB Design and manufacturing process. Design considerations for different types of PCBs – Single layer PCBs, Multilayer PCB, Flexible PCB etc. Design considerations for PCBs for different applications – digital circuits, Analog circuits, High speed circuits, Power circuits etc. Layout rules and parameters. Design rule checks – Signal layer checks, Power/Ground checks, Solder mask check, Drill check etc.

Manual verification – Thermal design, plane split width, isolation, PCB thickness etc. Automated processes, Through Hole vs SMT technologies. Thermal profiling during SMD/PTH assembly.

Case studies to understand DFM from design, manufacturing and Assembly.

Module 3 (10 Hours): Miniaturization and increased complexity of VLSI circuits Functional Yield, Parametric Yield, Reliability, Yield Loss Modules, Yield analysis Higher Yield Cells, Spacing and Width of interconnect wires, Redundancy in the design, Fault Tolerant vias, generation of yield optimized cells, layout compaction, wafer mapping optimization, planarity fill, statistical timing.

References:

1. Michael Orshansky, Sani Nassif, Duane Boning, *Design for Manufacturability And Statistical Design: Constructive Approach*, Springer, 2008
2. Chiang, Charles, Kawa, Jamil, *Design for Manufacturability and Yield for Nano-Scale CMOS*, Springer 2007
3. R S Khandpur, *Printed Circuit Boards*, Tata McGraw-Hill, 2005

EC6131D ARTIFICIAL INTELLIGENCE

Pre-requisites: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Find appropriate idealizations for converting real world problems into AI search problems

CO2: Implement heuristic and iterative deepening search algorithms

CO3: Invent knowledge representation in different formats

CO4: Advocate machine learning as an integral part of AI

Module 1: (16 hours)

Artificial Intelligence: History and Applications, Production Systems, Structures and Strategies for state space search- Data driven and goal driven search, Depth First and Breadth First Search, DFS with Iterative Deepening, Heuristic Search- Best First Search, A* Algorithm, AO* Algorithm, Local Search Algorithms and Optimization Problems, Constraint satisfaction, Using heuristics in games- Minimax Search, Alpha Beta Procedure. Implementation of Search Algorithms in LISP.

Languages and Programming Techniques for AI- Introduction to PROLOG and LISP, Search strategies and Logic Programming in LISP, Production System examples in PROLOG

Module 2:(13 hours)

Knowledge representation - Propositional calculus, Predicate Calculus, Forward and Backward chaining, Theorem proving by Resolution, Answer Extraction, AI Representational Schemes- Semantic Nets, Conceptual Dependency, Scripts, Frames, Introduction to Agent based problem solving. Implementation of Unification, Resolution and Answer Extraction using Resolution.

Module 3: (10 hours)

Machine Learning- Symbol based and Connectionist, Social and Emergent models of learning, Planning- Planning and acting in the real World, The Genetic Algorithm- Genetic Programming, Overview of Expert System Technology- Rule based Expert Systems, Introduction to Natural Language Processing. Implementation of Machine Learning algorithms.

References:

1. George F Luger, *Artificial Intelligence - Structures and Strategies for Complex Problem Solving*, 4/e, 2002, Pearson Education.
2. E. Rich and K.Knight, *Artificial Intelligence*, 2/e, Tata McGraw Hill
3. S Russel and P Norvig, *Artificial Intelligence - A Modern Approach*, 2/e, Pearson Education, 2002
4. Nils J Nilsson, *Artificial Intelligence a new Synthesis*, Elsevier, 1998
5. Ivan Bratko, *Prolog Programming for Artificial Intelligence*, 3/e, Addison Wesley, 2000
6. Dr.RussellEberhart and Dr.Yuhuishi, *Computational Intelligence - Concepts to Implementation*, Elsevier, 2007
7. Fakhreddine O Karray, Clarence De Silva, *Soft Computing and Intelligent Systems Design- Theory tools and Applications*, Pearson Education, 2009.

EC6132D DATA STRUCTURES AND ALGORITHMS

Pre-requisite: Nil

L	T	P	C
3	0	0	3

Total hours: 39

Course Outcomes:

CO1: Analyze different algorithms in terms of their space and time complexity.

CO2: Model systems as classes to enable ease of problem solving

CO3: Identify problems and model them as trees and graphs

CO4: Assess and compare different sorting algorithms

Module 1: (13 hours)

General concepts of object oriented programming C++, Class overview-Class Definition, Access Control, Class Scope, Constructors and Destructors, Inheritance, Polymorphism, Overloading, Encapsulation, Friend functions, dynamic memory allocation and de-allocation. Complexity analysis, asymptotic notation, Recursion. Sorting algorithms: Selection Sort, Quick sort, Merge Sort. Abstract data types -Linked lists, Stack and Queue. Searching: Linear and Binary search implementation. Implementation of sorting, searching, linked lists, stack and queues using C++

Module 2: (13 hours)

Binary tree - in-order, pre-order and post-order traversals – representation and evaluation of arithmetic expressions using binary tree, Binary Search trees - insertion, deletion and search- Prefix, Infix and Post fix representation and conversions,-Heaps and heap sort. Implementation of tree algorithms using C++

Module 3: (13 hours)

Graph representation - Adjacency matrix, Adjacency lists - Depth First Search (DFS) - Breadth First Search (BFS), Minimum spanning tree problem - Kruskal's algorithm - Prim’s algorithm Shortest path problem - Dijkstra's algorithm - Implementation of graph algorithms using C++and the Standard Template library Hashing - chaining – linear probing – double hashing

References:

1. D.Ravichandran, *Programming with C++*, Third Edition, Mc Graw Hill Education, 2011
2. D.Corman, Charles E. Leiserson, Ronald L. Rivest, *Introduction to Algorithms*, Third Edition, MIT, 2009.
3. Yedidyah Langsam, Moshe J. Augenstein, Aaron M. Tanenbaum, *Data Structures using C++*, Pearson Education, 2016
4. Larry Nyhoff, ADTs, *Data Structures and Problem Solving with C++*, Second Edition, Pearson Education, 2012
5. Sahni S., *Data Structures, Algorithms, and Applications in C++*, Mc Graw Hill, Singapore, 1998.

EC6133D ELECTRONIC PACKAGING

Pre-requisites: Nil

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3	0	0	3

Total Hours: 39

Course Outcomes:

CO1: Illustrate Electronic packaging and examine problems/solutions involved in materials/electrical aspects of it.

CO2: Elaborate various IC/systems packaging techniques and assess their suitability in application areas.

CO3: Inspect electronic package for reliability, thermal management and testability.

CO4: Assess new trends in packaging.

Module 1: (12 hours)

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology.

Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging.

Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference.

Module 2: (16 hours)

IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging. Different types of IC packages – DIP,QFP,etc.

Systems Packaging – MCM /SoC/SiP/SoP.

Discrete, Integrated and Embedded Passives.

Printed Circuit Board – Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards.

Board Assembly – Surface Mount Technology, Through-Hole Technology, Process Control and Design challenges.

Module 3: (11 hours)

Design for Reliability – Fundamentals, Induced failures.

Thermal Management for IC and PWBs, Cooling Requirements, Electronic cooling methods.

Electrical Testing – System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability, Trends in packaging.

References:

1. Rao R. Tummala, *Fundamentals of Microsystem Packaging*McGraw Hill,2001.
2. Richard K. Ulrich &William D. Brown *Advanced Electronic Packaging* - 2nd Edition : IEEEPress, 2006.
3. Rao R. Tummala, MadhavanSwaminathan, *Introduction to System-on-Package (SOP)*, McGraw-Hill, 2008.