CURRICULUM AND SYLLABUS OF M. TECH. DEGREE PROGRAMME IN MICROELECTRONICS & VLSI DESIGN
(Applicable from 2018 admission onwards)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY CALICUT
Vision of the Department of Electronics and Communication Engineering

The Department of Electronics and Communication Engineering is envisioned to be a leading centre of higher learning with academic excellence in the field of electronics and communication engineering.

Mission of the Department

The mission of the Department of Electronics and Communication Engineering is to impart high quality technical education by offering undergraduate, graduate and research programs in the domain of Electronics and Communication Engineering with thorough foundation in theory along with strong hands-on design and laboratory components, tools and skills necessary for the students to become successful major contributors to society and profession.

PEOs and Programme Outcomes: PG EC 62 :Microelectronics and VLSI Design

Programme Educational Objectives (PEOs):

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<tr>
<th>Sl. No.</th>
<th>Program Educational Objectives</th>
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<tbody>
<tr>
<td>PEO 1</td>
<td>To provide graduates strong theoretical foundation in the area of Microelectronics and VLSI Design and enable them to take up the challenges of the current technology.</td>
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<tr>
<td>PEO 2</td>
<td>To impart research skills with the aid of modern TCAD tools so that graduates can come up with solutions to the challenging problems in the area of Microelectronics and VLSI Design and formulate innovative ideas through independent thinking and Reflective Learning</td>
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<tr>
<td>PEO 3</td>
<td>To impart research skills and encourage continuous learning and improvement in the area of Microelectronics &amp; VLSI Design so that the graduates feel confident enough to face the challenges of the rapidly changing global scenario.</td>
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<tr>
<td>PEO 4</td>
<td>To upkeep the highest values of professionalism and ethical attitude and nurture the ability to relate engineering issues to broader social context.</td>
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Programme Outcomes (POs)

The student who completes the Master of Technology in Microelectronics and VLSI Design will be able to

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<th>Sl. No.</th>
<th>Program Outcome</th>
<th>Graduate Attribute</th>
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<tr>
<td>PO 1</td>
<td>Acquire in-depth knowledge in the broad area of Microelectronics and VLSI Design and allied disciplines, with an ability to discriminate, evaluate, analyze and synthesize the acquired knowledge.</td>
<td>Scholarship of Knowledge</td>
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<tr>
<td>PO 2</td>
<td>Analyze complex problems in the domain of Microelectronics and VLSI Design critically to make intellectual and creative advances for conducting research in a wider, theoretical, and practical and policy context.</td>
<td>Critical Thinking</td>
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<td>PO 3</td>
<td>Solve problems in the area of Microelectronics and VLSI Design imparting lateral thought and originality.</td>
<td>Problem Solving</td>
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<td>PO 4</td>
<td>Develop skills to extract information on research problems through literature survey and apply appropriate research methodologies, techniques and tools to design and conduct experiments, analyze and interpret data and demonstrate higher order skills to contribute individually or in groups to the development of scientific or technological knowledge Microelectronics and VLSI Design.</td>
<td>Research Skill</td>
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<tr>
<td>PO 5</td>
<td>Model and simulate problems in the area of Microelectronics &amp; VLSI Design by using modern tools and interpret the data to propose innovative ideas.</td>
<td>Usage of Modern Tools</td>
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<tr>
<td>PO 6</td>
<td>Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research in the area of Microelectronics and VLSI Design.</td>
<td>Collaborative and Multidisciplinary Work</td>
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<td>PO 7</td>
<td>Demonstrate knowledge and understanding of engineering and management principles and apply the same to one’s own work, as a member and leader in a team, with due consideration of economical and financial factors in the area of Microelectronics &amp; VLSI Design.</td>
<td>Project Management and Finance</td>
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<td>PO 8</td>
<td>To express ideas with clarity and communicate confidently and effectively to the international community through reports adhering to appropriate standards and/or oral presentations using audio and / video supplements.</td>
<td>Communication</td>
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<td>PO 9</td>
<td>Recognize the need to engage in life-long learning with a high level of enthusiasm and commitment to improve knowledge in the domain of Microelectronics and VLSI Design.</td>
<td>Life-long Learning</td>
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<td>PO 10</td>
<td>Acquire professional and intellectual integrity, professional code of conduct and ethics of research, considering the impact of research outcome on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.</td>
<td>Ethical Practices and Social Responsibility</td>
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<td>PO 11</td>
<td>Independently and critically analyze and make corrective measures for continuous improvement, without external feedback.</td>
<td>Independent and Reflective Learning</td>
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# Curriculum for M. Tech. EC62 Microelectronics and VLSI Design

## Semester 1

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Notes

1. A minimum of 60 credits have to be earned for the award of M. Tech Degree in this Programme.
2. A minimum of three elective courses is to be credited from the list of electives specified for the stream with the consent of the respective faculty.
3. A maximum of two theory electives can be credited from any other specializations, offered by the institute at M. Tech. level, with the consent of the HOD, the Programme Coordinator and the Course Faculty.
EC6201D DIGITAL INTEGRATED CIRCUIT DESIGN

Pre-requisites: Nil

Total hours: 39L + 26P

Course Outcomes:

CO1: Calculate various parameters and short channel effects of a MOSFET
CO2: Derive static and dynamic characteristics of digital CMOS circuits
CO3: Design and simulate static and dynamic CMOS logic circuits for a given functionality and speed, power consumption and area requirements
CO4: Design SRAM and DRAM cells using CMOS

Module 1: (10 hours)

Review of MOSFET threshold voltage, current, channel length modulation, body bias effect, Scaling and short channel effects, latch up effect, MOS switch, MOSFET capacitances, CMOS layout elements, parasitics, wires and vias - design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Module 2: (14 hours)

CMOS inverter, static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, Simulation of static and dynamic characteristics, layout, post layout simulation

Module 3: (15 hours)

Static CMOS design, Complementary MOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS – Course project

CMOS memory design – SRAM, DRAM and CAM memory design

References:

EC6202D ANALOG INTEGRATED CIRCUIT DESIGN

Pre-requisites: Nil

Total hours: 39L + 26P

Course Outcomes:

CO1: Model various components in CMOS process to estimate their performance in circuits.

CO2: Obtain the design of the biasing circuits for CMOS amplifiers.

CO3: Design single stage amplifiers and various stages of an operational amplifier.

CO4: Design fully differential amplifiers and comparators

Module 1: (10 hours)

Components available in a CMOS process; Resistors; Random and systematic mismatch; Layout techniques to minimize mismatch, Resistor model; Capacitors, MOS transistor layout; 4 terminal MOS transistor model; Threshold voltage, Drain current, Body bias effect, Channel length modulation, Influence of body effect on small and large signal behaviour of basic amplifier circuits, Small signal model of the MOS transistor; Low frequency MOSFET model, High frequency MOSFET model, Transit frequency, MOS transistor mismatch; Noise, Basics of noise-variance, autocorrelation, spectral density; Resistor noise, kT/C across a capacitor; MOS transistor noise, MOS transistor thermal and flicker noise

Module 2: (16 hours)

Current sources and sinks, Current mirrors, Matching considerations in current mirrors, Concept of current steering, Self biasing circuits, Constant Gm biasing, Start-up circuits, Bandgap referenced biasing, voltage references

Single transistor amplifiers – Telescopc Cascode amplifier, Folded cascade amplifier, Differential amplifier Noise in amplifiers, Input referred noise - Operational amplifiers - Frequency response of the amplifiers Negative feedback and stability, loop gain and unity loop gain frequency, feedback compensation, opamp offset, swing limits, slew rate, Design of single stage and multistage Operational amplifiers- Noise in operational amplifier, Effect of transistor mismatches in the performance of amplifiers

Module 3: (13 hours)

Fully differential opamps, Analysis of fully differential circuits using common-mode and differential half circuits, common mode feedback, CMFB circuits, Common mode feedback loop stability, Fully differential two stage opamp

CMOS comparator, comparator parameters: Sensitivity, Offset, speed, power dissipation, power supply rejection, input capacitance, kickback noise, Metastability, input CM range, Comparator design issues, Offset cancellation, Correlated Double sampling, Differential comparators, Latches, Pre amplifier stages.

References:

EC6203D ADVANCED SEMICONDUCTOR DEVICE MODELING

Pre-requisites: Nil

Total hours: 39L + 26P

Course Outcomes:

CO1: Apply the qualitative understanding of physics of semiconductors to develop quantitative models for semiconductor phenomena relevant to the field of electronics.

CO2: Model semiconductor homo junction and characterize p-n junction diodes

CO3: Analyze metal semiconductor junctions and model Metal oxide semiconductor junctions

CO4: Interpret and Model Metal oxide semiconductor FETs.

Module 1: (15 hours)


Module 2: (10 hours)

Semiconductor homo junctions – Analysis of p-n junction under equilibrium and bias – energy band diagram – diode current equation – break down of p-n junctions – Metal semiconductor junction – TCAD simulation of p-n junction diodes

Module 3: (14 hours)

Metal oxide semiconductor junction – Capacitance - voltage characteristics – threshold voltage – effect of work function difference and insulator charges

Metal Oxide Semiconductor Field effect transistors – Current–voltage characteristics – Sub threshold operation- Substrate bias effects – short channel effects and MOSFET scaling

TCAD simulation of MOS capacitor and MOSFETs.

References:

EC6204D VLSI TECHNOLOGY

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Outline the basics of semiconductor crystal properties.
CO2: Identify the fundamentals of IC fabrication.
CO3: Illustrate the advanced methods involved in photolithography.
CO4: Build an idea on process integration – NMOS, CMOS and Bipolar process.

Module 1: (13 hours)
Material properties, crystal structure, lattice, basis, planes, directions, angle between different planes, phase diagram and solid solubility, Crystal growth techniques, Epitaxy, Clean room and safety requirements. Oxidation: wet and dry oxidation, Deal-Grove model, Diffusion process, Ion implantation, modeling of Ion implantation, statistics of ion implantation, rapid thermal annealing, SIMS.

Module 2: (15 hours)
Deposition & Growth: Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating, LPCVD, MBE, ALCVD, Growth of High k and low k dielectrics, Etching - wet and dry etch, plasma and RIE etch, Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, resolution, depth of focus, numerical aperture sensitivity, contrast, proximity and projection lithography, step and scan, optical proximity correction.

Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL

Module 3: (11 hours)
Planarization Techniques: Need for planarization, Chemical Mechanical Polishing

Copper damascene process; Multi-level metallization schemes, Process integration: Bipolar process, NMOS and CMOS.

References:

EC6205D PHYSICAL DESIGN AUTOMATION

Pre-requisites: Nil

Total hours: 39L + 26P

Course Outcomes:

CO1: Identify the issues at various stages of VLSI physical design.

CO2: Develop algorithms to solve the complex physical design problems in ICs.

CO3: Analyze and optimize the algorithms that help in the back end design of complex chips.

CO4: Apply physical design techniques and design an IC for specific area, delay and power requirements.

Module 1: (12 hours)

Introduction to digital IC design - custom and semicustom flow, combinational logic synthesis - Technology independent and technology dependent optimization - Binary decision diagrams - High level synthesis - Scheduling and allocation – Physical design – terminology - graph algorithms – heuristic algorithms – Basic Unix/Linux commands – introduction to C shell/Perl scripting.

Module 2: (13 hours)


Module 3: (14 hours)


References:

EC6205D SEMINAR

Pre-requisites: Nil

Total Hours: 26

Course Outcomes:

CO1: Survey the literature on new research areas and compile findings on a particular topic

CO2: Organize and illustrate technical documentation with scientific rigor and adequate literal standards on the chosen topic strictly abiding by professional ethics while reporting results and stating claims.

CO3: Demonstrate communication skills in conveying the technical documentation via oral presentations using modern presentation tools.

The objective of the seminar is to impart training to the students in collecting materials on a specific topic in the broad domain of Engineering/Science from books, journals and other sources, compressing and organizing them in a logical sequence, and presenting the matter effectively both orally and as a technical report. The topic should not be a replica of what is contained in the syllabi of various courses of the M. Tech program. The topic chosen by the student shall be approved by the Faculty-in-Charge of the seminar. The seminar evaluation committee shall evaluate the presentation of students. A seminar report duly certified by the Faculty-in-Charge of the seminar in the prescribed form shall be submitted to the department after the approval from the committee.
EC7201D PROJECT: PART 1

Pre-requisites: Nil

Total Hours: 312

Course Outcomes:

CO1: Develop aptitude for research and independent learning.

CO2: Demonstrate the ability to carry out literature survey and select unresolved problems in the domain of the selected project topic.

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4: Acquire the knowledge and awareness to carry out cost-effective and environment friendly designs.

CO5: Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals.

The major project in the third and fourth semesters offer the opportunity to apply and extend knowledge acquired in the first year of the M. Tech. program. The major project can be analytical work, simulation, hardware design or a combination of these in the emerging areas of Microelectronics and VLSI Design under the supervision of a faculty from the ECE Department. The specific project topic undertaken will reflect the common interests and expertise of the student(s) and supervisor. Students will be required to 1) perform a literature search to review current knowledge and developments in the chosen technical area; 2) undertake detailed technical work in the chosen area using one or more of the following:

- Analytical models
- Computer simulations
- Hardware implementation

The emphasis of major project shall be on facilitating student learning in technical, project management and presentation spheres. Project work will be carried out individually. The M. Tech. project evaluation committee of the department shall evaluate the project work during the third semester in two phases. The first evaluation shall be conducted in the middle of the semester. This should be followed by the end semester evaluation. By the time of the first evaluation, students are expected to complete the literature review, have a clear idea of the work to be done, and have learnt the analytical / software / hardware tools. By the time of the second evaluation, they are expected to present the results of their advancements in the chosen topic, write an interim technical report of the study and results and clearly state the work plan for the next semester.
EC7202D PROJECT: PART 2

Pre-requisites: Successful completion of EC7201D Project: Part 1

Total Hours: 338

Course Outcomes:

CO1: Develop aptitude for research and independent learning.

CO2: Demonstrate the ability to carry out literature survey and select unresolved problems in the domain of the selected project topic.

CO3: Gain the expertise to use new tools and techniques for the design and development.

CO4: Acquire the knowledge and awareness to carry out cost-effective and environment friendly designs.

CO5: Develop the ability to write good technical report, to make oral presentation of the work, and to publish the work in reputed conferences/journals.

EC7202D Project: Part 2 is a continuation of EC7201D Project: Part 1 in the third semester. Students should complete the work planned in the third semester, attaining all the objectives, and should prepare the project report of the complete work done in the two semesters. They are expected to communicate their innovative ideas and results in reputed conferences and/or journals. The M. Tech. project evaluation committee of the department shall evaluate the project work during the fourth semester in two phases. The first evaluation shall be conducted towards the end of the semester. This should be followed by a second evaluation by the committee including an external examiner.
EC6211D MOS DEVICE MODELING

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Apply the qualitative understanding of Metal oxide Semiconductor system to derive quantitative models for potential -charge relation and capacitance effects.

CO2: Model the body bias effects on the operation of an MOS system.

CO3: Analyze the physics of four terminal MOS system and interpret the current voltage relation of a Metal oxide semiconductor field effect transistor.

CO4: Model the small channel and thin oxide effects in MOSFET operation.

Module 1: (12 hours)

Energy band diagram of MOS capacitor at equilibrium – Flat band voltage – Effect of application of gate to body voltage – accumulation, depletion, weak, moderate and strong inversion conditions – non ideal insulator – threshold voltage - capacitance voltage relation – The three terminal MOS structure – effect of body bias on surface conditions – Threshold voltage with body bias

Module 2: (12 hours)

The four terminal Metal Oxide Semiconductor transistor – strong inversion, moderate inversion and weak inversion current - voltage models – Effective mobility – Effect of source and drain series resistance – Temperature effects – Break down

Module 3: (15 hours)


References:

EC6212D ANALOG SYSTEM DESIGN

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Design op-amps for applications demanding high speed, low power and rail-to-rail swing
CO2: Make use of the knowledge on continuous time filters to realize discrete switched capacitor filters
CO3: Analyze simple and charge pump PLLs using linear models
CO4: Design sub blocks to meet the specifications of a PLL

Module 1: (12 hours)

Frequency compensation in feedback amplifiers, review of Miller compensation, feed forward topologies, Gain boosting in amplifiers, low power and low noise, low offset op-amps, high slew rate and fast settling op-amps, constant gm rail-to-rail input stage op-amps, output power efficiency, class AB biasing, output saturation protection and current limiting, analog circuit layout, op amp design using a SPICE tool

Module 2: (11 hours)

Resistor emulation using a MOSFET and capacitor, charge injection, clock feed-through, switched capacitor integrators, non-overlapping clock, switched capacitor gain circuits, first order and second order filters, switch sharing, low-Q and high-Q biquad filters, op-amps for switched capacitor circuits, Gm-C filters, CMOS transconductors, active RC and MOSFET-C filters, frequency and Q-factor tuning.

Module 3: (16 hours)

Operating principle of PLL, phase detector, XOR, JK FF and phase frequency detector, first order loop filters, voltage controlled oscillators, ring and LC oscillators, tuning range of VCOs, first order PLL, locked condition, transient response of PLL in the locked state, charge pump PLL, PFD/CP non-idealities, loop filter design, stability of the loop, fast lock technique, jitter in PLL, sources of noise in PLL, phase noise in PLL.

References:

EC6213D DIGITAL VLSI TESTING

Pre-requisites: Nil

Total hours: 39

Course Outcomes:
CO1: Develop test patterns required to detect faults in a circuit
CO2: Determine the testability of a circuit
CO3: Design methods/techniques to improve the testability of digital circuits.
CO4: Design Logic BIST circuits based on LFSRs

Module 1: (12 hours)
Introduction to VLSI Testing process, Fault models, Fault Collapsing, Logic Simulation and Fault simulation, Combinational Circuit Test Pattern Generation - Boolean Difference, Path Sensitization Methods, D-Algorithm, PODEM, Delay fault testing, IDDQ Testing

Module 2: (15 hours)
Combinational and Sequential SCOAP Measures, ATPG for Single-Clock Synchronous Circuits - Nine-Valued Logic and Time-Frame Expansion Methods, DFT based Sequential Circuit Testing - Adhoc design for testability - Test Point Insertion, Scan chains, Partial Scan Design, Random Access Scan, Boundary scan standard – Boundary scan cell, TAP controller, modes of operation, EXTEST, INTEST, BYPASS instructions

Module 3: (12 hours)
Built in Self-Test (BIST) - Exhaustive pattern generation, random pattern generation, LFSR for pattern generation and Output response analysis, SISR, MISR
Memory BIST – Type of memory faults, fault detection by MARCH tests
Issues in test and verification of complex chips, embedded cores and SOCs, System testing and test for SOCs

References:
EC6214D VLSI DIGITAL SIGNAL PROCESSING

Pre-requisites: Nil

Total hours: 39

Course Outcomes:
CO1: Identify the performance parameters of DSP implementation for hardware mapping
CO2: Apply different techniques to map DSP systems into reconfigurable logic/ASIC
CO3: Utilize the methods for the low power implementation of DSP algorithms
CO4: Design and implement multiplier-less DSP systems

Module 1: (15 hours)
Overview of DSP Filter structures - Recursive, Non-recursive and Lattice; Performance Measures of DSP implementation - Loop bound, Iteration period, critical path, Throughput, Latency, Power; Mapping DSP Systems into Reconfigurable Logic/ASIC – Retiming, pipelining, Parallel Processing; Hardware Sharing – Unfolding and Folding

Systolic Architecture Design – Systolic Array Design Methodology, FIR Systolic Arrays

Module 2: (12 hours)
Fast algorithms for DSP - Cook-Toom, Winograd, Iterated and Cyclic Convolution algorithms; Parallel FIR Filter structures

Finite Word Length Effects: Scaling, Round-off Noise and Coefficient Sensitivity

Low power realization of DSP algorithms, Weighted-sum computation and FIR Filters, Coefficient optimization, Circular buffer; Computational complexity and power analysis of multirate architectures, Power reduction using multirate architectures

Module 3: (12 hours)
Multiply Accumulator (MAC) - Distributed arithmetic based implementation, Techniques for Low Power Implementation of DA Based FIR Filters; Computation of Special Functions Using CORDIC

Multiplier-less implementation- Minimizing additions in weighted-sum and MCM computation, Common Sub-expression elimination, 2’s Complement representation, Canonical Signed Digit (CSD) representation.

References:
EC6215D COMPOUND SEMICONDUCTOR DEVICES AND APPLICATIONS

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Interpret important parameters governing the high speed performance of devices and circuits
CO2: Model the properties of Hetero junctions from the energy band diagram point of view
CO3: Model the Physics and operation and modeling of MESFETs
CO4: Interpret the operation and modeling of Hetero junction Bipolar Transistor

Module 1: (13 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature - Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices - Band diagrams, homo and hetero junctions

Module 2: (13 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current.

Module 3: (13 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET (MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices

References:

6. Ralph E. Williams, Modern GaAs Processing Methods, Artech House, 1990
EC6216D POWER SEMICONDUCTORS DEVICES AND TECHNOLOGY

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Interpret the physics of avalanche break down mechanism in power diodes
CO2: Model the applications of power BJT as a switch and explore typical switching applications
CO3: Explain Silicon power MOSFET theory and its applications
CO4: Model the operation of Silicon Carbide power MOSFET theory and its applications

Module 1: (10 hours)

Silicon power diodes - Avalanche Breakdown voltage of Silicon planar p-n junctions, Breakdown voltage improvement Techniques – Floating field rings – field plates - MESA structures.

High injection level effects in pn junctions. Forward voltage drop in high voltage PIN diodes - independence on carrier lifetime.

Module 2: (13 hours)

Silicon Bipolar Power Transistor structures and characteristics, Current-gain, Switching operation, second break down and safe operating area.

Silicon Power MOSFETs, I-V characteristics, on resistance, Minimum size chip design for specific drain breakdown voltage, Switching characteristics, Safe operating area, Insulated Gate Bipolar Transistor (IGBT) – Structure, Operation principle, I-V characteristics and turn off transients, Latch up and its prevention.

Module 3: (16 hours)

Silicon Carbide power Devices – Advantages of Silicon Carbide over Silicon from high power point of view – SiC Diodes – Avalanche Breakdown Voltage – SiC Power MOSFETs – Different SiC power MOSFET architectures – on state I-V characteristics – Break down voltage improvement - SiC IGBT

References:

EC6217 MEMS STRUCTURES AND APPLICATIONS

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Interpret the basic principle of micro sensors and actuators.

CO2: Demonstrate the basics of different micro machining technologies.

CO3: Develop knowledge on virtual fabrication based on different MEMS Simulators and different FEA tools

CO4: Analyze various bonding and packaging techniques in MEMS.

Module 1: (12 hours)

An introduction to Micro sensors and MEMS, Classical scaling in CMOS, Moore’s Law - Clean room concept, Evolution of Micro sensors & MEMS, Micro machined Micro sensors & MEMS applications: Mechanical, Inertial, Biological, Chemical, Acoustic, Integrated Smart Sensors

Module 2: (14 hours)

Microelectronic technologies for MEMS:- Oxidation: - concepts of wet and dry oxidation, Material deposition techniques:- evaporation, sputtering, CVD, PVD and MBE, Photolithography: - Positive and negative photoresists, proximity and projection lithography, Etching:- Isotropic and anisotropic etching, wet and dry etch, plasma etching, RIE etching, Micromachining :- Surface and Bulk Micromachining, general process description, problems associated to surface micromachining; LIGA process.

Module 3: (13 hours)

Microactuators: - Piezoelectric, chemical, Thermopneumatic, electrostatic and electromagnetic microactuators, MEMS Simulators and different FEA tools, Interface Electronics for MEMS, MEMS for RF Applications, Bonding & Packaging of MEMS- Direct bonding, Field assisted bonding, Bonding with an intermediate layer, General considerations in packaging design, The three levels of microsystem packaging, Packaging processing sequence, Conclusions & Future Trends.

References:

EC6218 CMOS IMAGE SENSORS

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Compare the performance of various pixels and choose suitable architecture for an application

CO2: Distinguish various noise sources in image sensors and estimate the noise of a signal path

CO3: Design building blocks of an image sensor readout

CO4: Develop architecture-dependent design optimizations in the readout of an image sensor

Module 1: (13 hours)

Review of MOS capacitor and MOSFET, charge transfer and charge coupled systems, floating diffusion nodes, effect of thermal, shot and trap-induced noises, limitation of CCDs, photo-generated charges, photodiode, photo current, photodiodes in a standard CMOS technology, readout architectures in CMOS technology, pixel circuits, passive and 3-T active pixels, fill factor, full well capacity, sensitivity, signal dependent non-idealities, reset, temporal and photon shot noise, signal-to-noise ratio, dynamic range, imager specifications from photon transfer curve

Module 2: (11 hours)

Readout architectures, pixel, column and chip level readouts, readout dependent fixed pattern noise, double sampling techniques, correlated double sampling, pinned-photodiode, 4-T active pixel, dark current and fixed pattern noise reduction, analog, digital and mixed mode CDS, column amplifier and sensitivity, adaptive gain column amplifiers, column fixed pattern noise reduction, the impact of transfer gate on full well capacity, high dynamic range pixels, logarithmic, linear-log pixel circuits, current mode and CTIA pixels, time mode pixels

Module 3: (15 hours)

Analog-to-digital converters in pixel, column and chip level operations, pixel pitch and speed of ADCs, comparators for ADCs, slope ADCs and accelerated-ramp slope ADCs, digital and continuous ramp generators, cyclic ADC, digital error correction, multi-step data converters, column shared architectures, technology scaling on pixels, pixel pitch reduction and the performance of ADCs, amplifier reusing and scaling of capacitors in cyclic ADCs, multiple sampling and noise canceling cyclic ADCs, SAR ADCs, pixel level ADCs, applications of CMOS image sensors, characterization of an image sensor

References:

EC6219D HIGH SPEED DIGITAL DESIGN

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Adapt to venture deep into the realm of high speed digital design

CO2: Relate to the inventory of wire models, noise, signaling and synchronization concepts associated with high speed design

CO3: Demonstrate an understanding of the concepts, thumb rules and design of basic high speed systems

CO4: Apply the understanding to the design of high speed systems and other allied fields appreciating the trade-offs between noise immunity, power, speed etc.

Module 1: (15 hours)

Modeling of interconnects - electrical models of wires, lumped single-element models, lumped multi-element models, transmission line model, thumb rules for the applicability of models

Power supply network – local regulation with bypass capacitors, regulation with active regulators, power supply isolation

Noise sources in digital system – Noise budgeting and SNR

Module 2: (12 hours)

Signalling modes for lumped-C medium, distributed RC medium and transmission lines - simultaneous bi-directional signalling - terminations

Transmitter circuits – full swing & low swing voltage drivers, current mode drivers, Gunning transceiver logic, rise-time control

Receiver circuits – voltage & time domain performance specifications, eye diagram, static and regenerative amplifiers, integrating receivers

Module 3: (12 hours)

Timing properties of clocked storage elements, open loop timing, level sensitive clocking, pipeline timing, closed loop timing

Off-chip and on-chip clock distribution, PLL and DLL based clock aligners

Synchronisation failure and metastability, probability of synchronization failure

Hierarchy of synchronizer design – delay line, 2-register and FIFO mesochronous synchronizers

References:

EC6220D LOW POWER VLSI

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Design CMOS circuits to reduce dynamic power dissipation
CO2: Identify different methods to reduce leakage power consumption in submicron technologies
CO3: Design low power random access memories and arithmetic circuits

Module 1: (14 hours)

Review of power dissipation in CMOS Circuits – sources of power dissipation - static, dynamic and leakage power dissipation -

Dynamic power reduction – Supply voltage scaling approaches: Optimal Transistor Sizing with Voltage Scaling, parallelism, pipelining, optimal supply voltage, using multiple supply voltage, multiple device threshold, Dynamic voltage and frequency scaling, feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization

Module 2: (13 hours)

Minimizing Switched Capacitance – Switching activity reduction, algorithmic optimization, architecture optimization, logic optimization, circuit optimization, Different logic styles – static and dynamic logic, Clock gating, reducing glitching through path balancing, input reordering

RTL Coding for low power – Glitch reduction, clock gating, gated clock FSM, precomputation, bus encoding

Module 3: (12 hours)

Leakage Reduction Techniques – Transistor stacks, power gating, Multi-Threshold CMOS, Variable-Threshold CMOS, Dynamic Threshold CMOS, Fabrication of multiple threshold voltages

Low-power CMOS Random Access Memory Circuits, Adiabatic circuits, Asynchronous system basics

References:

EC6221D VLSI DATA CONVERTERS

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Compare data converters' performance based on static and dynamic specifications
CO2: Design current steering DAC with suitable segmentation
CO3: Decide the Nyquist ADC architecture and develop the architecture that meets the performance specifications
CO4: Analyze oversampling Delta-Sigma ADCs with suitable models

Module 1: (10 hours)

Sampling, Non idealities in sampling, noise and distortion in sampling, sample and hold circuits, timing issues in sample and hold circuit, bootstrapping systems, charge injection and noise, introduction to switched capacitor circuits, switched capacitor sample and hold circuits, static specifications of data converters, accuracy, nonlinearity, offset, dynamic specifications, SNR, SFDR, ENOB, dynamic range

Module 2: (16 hours)

Digital-to-analog converter in voltage, current steering DAC, segmentation, static and dynamic errors, accuracy, calibration, dynamic element matching, decoders and matrix DAC architecture design, Flash ADC, impacts of latch meta-stability, kick-back noise and offset, sub ranging and pipeline converter architectures, 1.5 bit/stage and error correction, folding and interleaving architectures, SAR ADC

Module 3: (13 hours)

Oversampling and quantization noise spectrum, linearity with oversampling, first order noise shaping, delta sigma modulator with noise shaping, switched capacitor implementation, linearized analysis, stability of delta sigma modulators, decimation filters with accumulate and dump, averaging without decimation, aliasing, interpolation filters for DAC, second order noise shaping, linearity, idle tones and dithering, multi stage noise shaping architectures, error-feedback structures

References:

EC6222D CMOS RF IC DESIGN

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Adapt to venture deep into the RF spectrum
CO2: Relate to the inventory of RF device models
CO3: Demonstrate an understanding of the language, basic operation and design of basic RF modules
CO4: Apply the understanding to the design of wireless systems and other allied fields appreciating the trade-offs between noise, linearity, spectral cost etc.

Module 1: (13 hours)
Basics of RF circuit design - Noise: Available noise power, noise figure
Linearity & distortion: Third-order intercept point, second-order intercept point, 1-dB compression point, broadband measures of linearity - Modeling of active & passive components at high frequencies
Impedance matching: broadband matching, power matching & noise matching
High frequency amplifiers: bandwidth estimation using open-circuit & short-circuit time constants - using zeros to enhance bandwidth - shunt-series amplifiers, tuned amplifiers & cascaded amplifiers

Module 2: (13 hours)
RF power amplifiers: Design of class A, AB, B, C, D, E, F, G & H amplifiers - Low-noise amplifier (LNA).
CS, CG & cascode amplifiers, shunt-series feedback amplifiers, noise & linearity of amplifiers, amplifiers using differential configurations, Low voltage topologies for LNA, DC bias networks for LNA, design of broadband LNA
Mixers: Mixing operation, mixing with nonlinearity, mixer noise & linearity, mixer with local oscillator switching, popular mixer configurations like the Moore mixer, mixer with simultaneous noise and power match, mixer employing current reuse for low power applications

Module 3: (13 hours)
Oscillators: Negative resistance-based LC resonator, Colpitts oscillator, differential topologies, phase noise in oscillators, tunable oscillators
Phase-locked loops (PLL) & frequency synthesizers, PLL components, continuous-time and transient behavior of PLL, in-band and out-of-band phase noise
Frequency synthesizers: Integer-N & fractional-N synthesizers, spurious components in synthesizers

References:

EC6223D FOUNDATIONS OF VLSI CAD

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Identify the issues at various stages of IC design.
CO2: Develop algorithms to solve the complex design problems in ICs.
CO3: Optimize the algorithms so that it can handle the design of IC containing multi million transistors.
CO4: Demonstrate capability for CAD tool development and enhancement.

Module 1: (11 hours)


Module 2: (13 hours)

Graphs - representation of graphs using matrices; Paths, connectedness; circuits, cutsets, trees; Fundamental circuit and cutset matrices; Voltage and current spaces of a directed graph and their complementary orthogonality.

Module 3: (15 hours)

Algorithms and data structures: efficient representation of graphs; Elementary graph algorithms involving BFS and DFS trees, such as finding connected and 2-connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph - data structures such as stacks, linked lists and queues, binary trees and heaps - time and space complexity of algorithms - Algorithms for VLSI Physical Design - Synthesis, Circuit Simulation and Digital Design Automation.

References:

Department of Electronics and Communication Engineering, National Institute of Technology Calicut, 673601

EC6224 VERIFICATION OF VLSI SYSTEMS

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Estimate the effort required for verification and formulate a verification plan for complex IC designs.

CO2: Develop HVL based self-checking test benches both directed and random.

CO3: Apply techniques to assess the verification efficiency and identify the methods to improve it.

CO4: Select suitable formal verification methods for exhaustive verification of a design.

Module 1: (13 hours)


Module 2: (13 hours)


Module 3: (13 hours)


References:

EC6225D SOI DEVICE MODELING AND SIMULATION

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Develop and understanding of Silicon on Insulator Technology and different types of SOI MOSFET structures.

CO2: Investigate into various Technology aspects of Multiple Gate MOSFET Design.

CO3: Model the physics of Multiple Gate MOSFETs.

Module 1: (13 hours)

Silicon on insulator concept – partially depleted and fully depleted SOI MOSFETs – Advantages of SOI MOSFETs over bulk MOSFET – Single Gate, Double Gate, Triple Gate and surrounding gate SOI MOSFETs – Physics of multi gate SOI MOSFETs

Module 2: (13 hours)

Multiple Gate MOSFET Technology – Fin Design – Design of - Gate stack – source Drain Series Resistance and Capacitance – Mobility and strain Engineering – Contact to the Fins

Module 3: (13 hours)


References:

EC6121D ADVANCED EMBEDDED COMPUTING

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Identify the advanced architectural features of advanced Intel and ARM processors
CO2: Review and research the state of the art in internet protocols
CO3: Discuss and identify the latest short range, low power protocols
CO4: Estimate the relevance of the Linux OS and device drivers based on Linux

Module 1: (16 hours)


Module 2: (13 hours)


Module 3: (10 hours)

Linux and linux device drivers –Linux Internals-Project work on porting a real time OS onto an Embedded board

References:

EC6124D DESIGN FOR MANUFACTURABILITY

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Appraise the product manufacturing process, importance of manufacturer, different DFM rules and guidelines.

CO2: Summarize different types of PCBs and their design considerations for manufacturability.

CO3: Analyze the manufacturability of Integrated Circuits with various design constrains.

Module 1 (15 Hours):


Need for different DFM techniques for different companies – Different applications, Different manufactures, Different equipment and processes. Development of DFM rules, Design Guidelines, exceptions.

Simple assembly process vs complex and expensive components, Simple component manufacture vs complex manufacturing process, Simple and inexpensive design vs expensive and complex service and support.

DFM softwares. Emerging manufacturing trends, Lead free design, standard design processes, Certifications. Over view of Design for Testability, Design for Assembly, Design for serviceability, Design for reliability etc.

Module 2 (14 Hours):

PCB Design and manufacturing process. Design considerations for different types of PCBs – Single layer PCBs, Multilayer PCB, Flexible PCB etc. Design considerations for PCBs for different applications – digital circuits, Analog circuits, High speed circuits, Power circuits etc. Layout rules and parameters. Design rule checks – Signal layer checks, Power/Ground checks, Solder mask check, Drill check etc.


Case studies to understand DFM from design, manufacturing and Assembly.

Module 3 (10 Hours):

Miniaturization and increased complexity of VLSI circuits Functional Yield, Parametric Yield, Reliability, Yield Loss Modules, Yield analysis Higher Yield Cells, Spacing and Width of interconnect wires, Redundancy in the design, Fault Tolerant vias, generation of yield optimized cells, layout compaction, wafer mapping optimization, planarity fill, statistical timing.

References:

EC6131D ARTIFICIAL INTELLIGENCE

Pre-requisites: Nil

Total hours: 39

Course Outcomes:

CO1: Find appropriate idealizations for converting real world problems into AI search problems
CO2: Implement heuristic and iterative deepening search algorithms
CO3: Invent knowledge representation in different formats
CO4: Advocate machine learning as an integral part of AI

Module 1: (16 hours)


Languages and Programming Techniques for AI- Introduction to PROLOG and LISP, Search strategies and Logic Programming in LISP, Production System examples in PROLOG

Module 2: (13 hours)


Module 3: (10 hours)


References:

2. E. Rich and K.Knight, Artificial Intelligence, 2/e, Tata McGraw Hill
5. Ivan Bratko, Prolog Programming for Artificial Intelligence, 3/e, Addison Wesley, 2000
6. Dr.RussellEberhart and Dr.Yuhuishi, Computational Intelligence - Concepts to Implementation, Elsevier, 2007
EC6132D DATA STRUCTURES AND ALGORITHMS

Pre-requisite: Nil

Total hours: 39

Course Outcomes:

CO1: Analyze different algorithms in terms of their space and time complexity.
CO2: Model systems as classes to enable ease of problem solving
CO3: Identify problems and model them as trees and graphs
CO4: Assess and compare different sorting algorithms

Module 1: (13 hours)


Module 2: (13 hours)


Module 3: (13 hours)

Graph representation - Adjacency matrix, Adjacency lists - Depth First Search (DFS) - Breadth First Search (BFS), Minimum spanning tree problem - Kruskal's algorithm - Prim's algorithm Shortest path problem - Dijkstra's algorithm - Implementation of graph algorithms using C++and the Standard Template library Hashing - chaining – linear probing – double hashing

References:

EC6133D ELECTRONIC PACKAGING

Pre-requisites: Nil

Total Hours: 39

Course Outcomes:

CO1: Illustrate Electronic packaging and examine problems/solutions involved in materials/electrical aspects of it.

CO2: Elaborate various IC/systems packaging techniques and assess their suitability in application areas.

CO3: Inspect electronic package for reliability, thermal management and testability.

CO4: Assess new trends in packaging.

Module 1: (12 hours)

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology.


Module 2: (16 hours)

IC Assembly – Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging. Different types of IC packages – DIP,QFP, etc.

Systems Packaging – MCM /SoC/SiP/SoP.

Discrete, Integrated and Embedded Passives.

Printed Circuit Board – Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards.


Module 3: (11 hours)

Design for Reliability – Fundamentals, Induced failures.

Thermal Management for IC and PWBs, Cooling Requirements, Electronic cooling methods.


References: